CA-IS308x 5kV$_{RMS}$ Isolated Half/Full-Duplex RS-485/RS-422 Transceiver

1. Features

- **High-Performance and Compliant with RS-485 EIA/TIA-485 Standard**
  - Up to 10Mbps data rate
  - The CA-IS3080/86 feature 1/8 unit load and enable up to 256 nodes on the bus
  - The CA-IS3082/88 allow up to 50 transceivers on the bus
  - 2.5V to 5.5V logic side supply voltage and 3.0 V to 5.5 V bus side supply voltage
  - 5kV$_{RMS}$ withstand isolation voltage for 60s (galvanic isolation)
  - ±150kV/µs typical CMTI
  - High lifetime: >40 years
  - ±8kV Human Body Model (HBM) ESD protection on bus I/O, ±4kV HBM ESD protection on logic I/O
  - Wide common-mode voltage range:
    CA-IS3080/86: -15V to +15V
    CA-IS3082/88: -7V to +12V
  - Current-limiting and thermal shutdown for driver overload protection
  - True fail-safe guarantees known receiver output state
- **Wide operating temperature range: –40°C to 125°C**
- **Wide-body SOIC16-WB(W) Package**
- **Safety Regulatory Approvals**
  - VDE 0884-11 and DIN EN & IEC 62368-1 VDE reinforced isolation (pending)
  - UL according to UL1577
  - IEC 62368-1, IEC 61010-1, GB 4943.1-2011 and GB 8898-2011, CQC reinforced insulation certifications

2. Applications

- Industrial Automation Equipment
- Grid infrastructure
- Solar inverter
- Motor drivers
- HVAC

3. General Description

The CA-IS308x family of devices is a galvanically-isolated RS-485/RS-422 transceiver that has superior isolation and RS485 performance to meet the needs of the industrial applications. All devices of this family have the logic input and output buffers separated by a silicon oxide (SiO_2) insulation barrier that provides up to 5000V$_{RMS}$ (60s) of galvanic isolation and ±150kV/µs typical CMTI. Isolation improves communication by breaking ground loops and reduces noise where there are large differences in ground potential between ports.

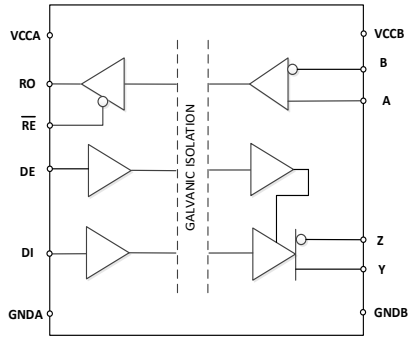
The CA-IS308x family of devices is designed for high-speed (up to 10Mbps) multidrop operation with high ESD protection of up to ±8kV HBM and ±12kV IEC 61000-4-2 Contact Discharge ESD protection. The receiver of CA-IS3080/86 is 1/8-unit load, allowing up to 256 transceivers (loads) on a common bus; while the CA-IS3082/88 feature lower input resistance(20kΩ, minimum) and allow up to 50 transceivers on the bus. Maintaining multidrop operation and increasing the maximum data rate offer a more robust system design for reliable communication. The CA-IS3080 and CA-IS3086 full-duplex transceivers are designed for bidirectional data communications on multipoint bus transmission lines simultaneously. The CA-IS3082 and CS-IS3088 provide half-duplex transceivers, the driver and receiver enable pins let any node at any given moment be configured in either transmit or receive mode which decreases cable requirements.

The CA-IS308x series devices are available in wide-body 16-pin SOIC package which is the industry standard isolated RS-485/RS-422 package, and operate over -40°C to +125°C temperature range.

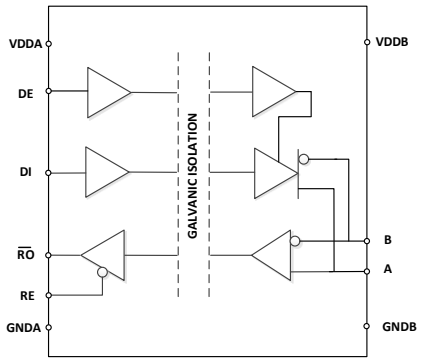
Device information

Part #	Package	Package size (NOM)
CA-IS3080	SOIC16-WB(W)	10.30 mm × 7.50 mm
CA-IS3082		
CA-IS3086		
CA-IS3088		

CA-IS3080/CA-IS3086 full-duplex block diagram



CA-IS3082/CA-IS3088 half-duplex block diagram



4. Ordering Information

Table 4-1. Ordering Information

Part #	V_{DDA}（V）	V_{DDB}（V）	Full/half-duplex	Transmission speed (mbps)	Rated voltage (V)	Package
CA-IS3080WX	2.5~5.5	3.0~5.5	Full-duplex	0.5	5000	SOIC16-WB
CA-IS3086WX	2.5~5.5	3.0~5.5	Full-duplex	10	5000	SOIC16-WB
CA-IS3082WX	2.5~5.5	3.0~5.5	Half-duplex	0.5	5000	SOIC16-WB
CA-IS3082WNX	2.5~5.5	3.0~5.5	Half-duplex	0.5	5000	SOIC16-WB
CA-IS3088WX	2.5~5.5	3.0~5.5	Half-duplex	10	5000	SOIC16-WB

Contents

5. Revision History

Revision Number	Description	Page Changed
Version 1.00	N/A	N/A
Version 1.01	The driver output changed to high-impedance state under thermal shutdown.	11
Version 1.02	Changed V_{IORM} to 1414V, $V_{IOWM}$to 1000V,V_{IOTM} to 1414V. Changed CA-IS3082W/WX/WNX,CA-IS3088W/WX electrical parameters. Added part number CA-IS3082WNX	8 10,12 2,6,23
Version 1.03	Removed CA-IS3080W, CA-IS3082W, CA-IS3086W and CA-IS3088W parts. Added CA-IS3080WX and CA-IS3086WX parts and relevant information. Changed V_{DDB} supply range to “3.0V ~ 5.5V”. Changed the common-mode voltage range of the CA-IS3080/86WX to ”-15V to +15V”.	1, 2

6. Pin Configuration and Description

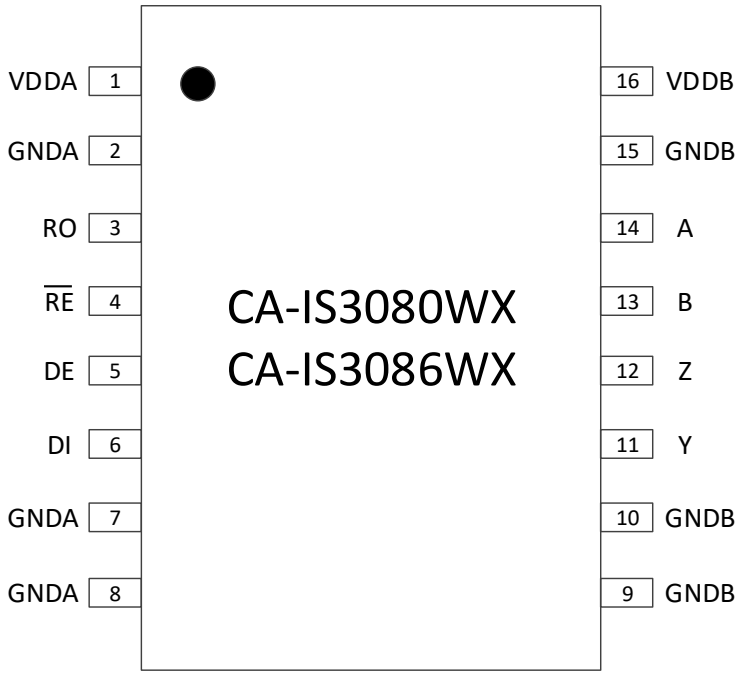


Figure 6-1. CA-IS3080WX and CA-IS3086WX Top View

Table 6-1. CA-IS3080WX and CA-IS3086WX Pin Description

Pin name	Pin number	Type	Description
VDDA	1	Power supply	Logic-Side Power Input. Bypass VDDA to GNDA with both 0.1μF and 1μF capacitors as close to the device as possible.
GNDA	2, 7 , 8	Ground	Logic-Side Ground. GNDA is the ground reference for digital signals.
RO	3	Digital I/O	Receiver Data Output. Drive $\overline{RE}$ low to enable receiver RX. With $\overline{RE}$ low, RO is high when (V_A –V_B) > -20mV and is low when (V_A – V_B) < -200mV.
$\overline{RE}$	4	Digital I/O	Receiver Output Enable. Driver $\overline{RE}$ low or connect to GNDA to enable RX. Drive $\overline{RE}$ high to disable RX, and out the receiver output at high-impedance.
DE	5	Digital I/O	Driver Output Enable. Drive DE high to enable bus driver outputs. Drive DE low or connect to GNDA to disable bus driver outputs. DE has an internal weak pull-down to GNDA.
DI	6	Digital I/O	Driver Input. With DE high, a logic low on DI forces the noninverting output (Y) low and the inverting output (Z) high; a logic high on DI forces the noninverting output high and the inverting output low.
GNDB	9, 10, 15	Ground	Cable Side Ground. GNDB is the ground reference for the RS-485/RS-422 bus signals.
Y	11	Bus I/O	Non-inverting RS-485/RS-422 driver output .
Z	12	Bus I/O	Inverting RS-485/RS-422 driver output.
B	13	Bus I/O	Inverting RS-485/RS-422 receiver input.
A	14	Bus I/O	Non-inverting RS-485/RS-422 receiver input.
VDDB	16	Power supply	Cable Side Power Input. Bypass VDDB to GNDB with both 0.1μF and 1μF capacitors as close to the device as possible.

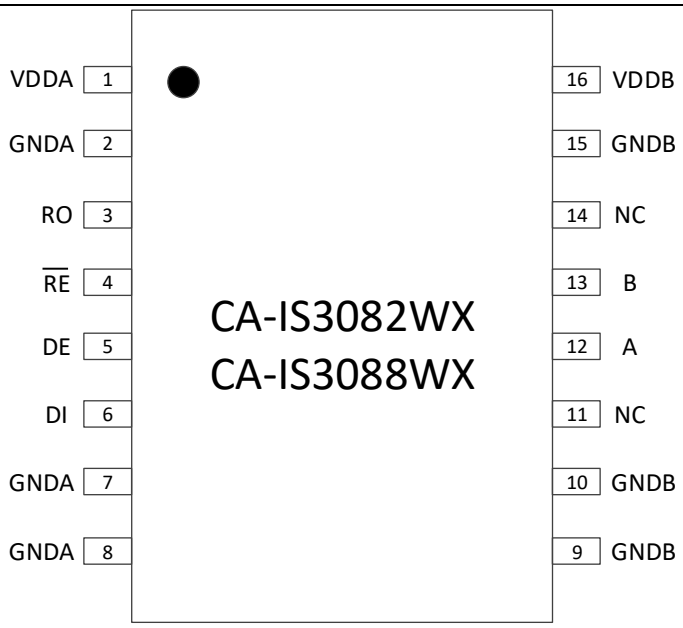


Figure 6-2. CA-IS3082WX and CA-IS3088WX Top View

Table 6-2. CA-IS3082WX and CA-IS3088WX Pin Description

Pin name	Pin number	Type	Description
VDDA	1	Power supply	Logic-Side Power Input. Bypass VDDA to GNDA with both 0.1μF and 1μF capacitors as close to the device as possible.
GNDA	2, 7, 8	Ground	Logic-Side Ground. GNDA is the ground reference for digital signals.
RO	3	Digital I/O	Receiver Data Output. Drive $\overline{RE}$ low to enable receiver (RX). With $\overline{RE}$ low, RO is high when (V_A –V_B) > -20mV and is low when (V_A – V_B) < -200mV.
$\overline{RE}$	4	Digital I/O	Receiver Output Enable. Drive $\overline{RE}$ low or connect to GNDA to enable receiver (RX). Drive $\overline{RE}$ high to disable RX.
DE	5	Digital I/O	Driver Output Enable. Drive DE high to enable bus driver outputs. Drive DE low or connect to GNDA to disable bus driver outputs. DE has an internal weak pull-down to GNDA.
DI	6	Digital I/O	Driver Input. With DE high, a logic low on DI forces the noninverting output (A) low and the inverting output (B) high; a logic high on DI forces the non-inverting output high and the inverting output low.
GNDB	9, 10, 15	Ground	Cable Side Ground. GNDB is the ground reference for the RS-485/RS-422 bus signals.
NC	11, 14	-	No internal connection
A	12	Bus I/O	Non-inverting RS-485/RS-422 receiver input and driver output.
B	13	Bus I/O	Inverting RS-485/RS-422 receiver input and driver output.
VDDB	16	Power supply	Cable Side Power Input. Bypass VDDB to GNDB with both 0.1μF and 1μF capacitor as close to the device as possible.

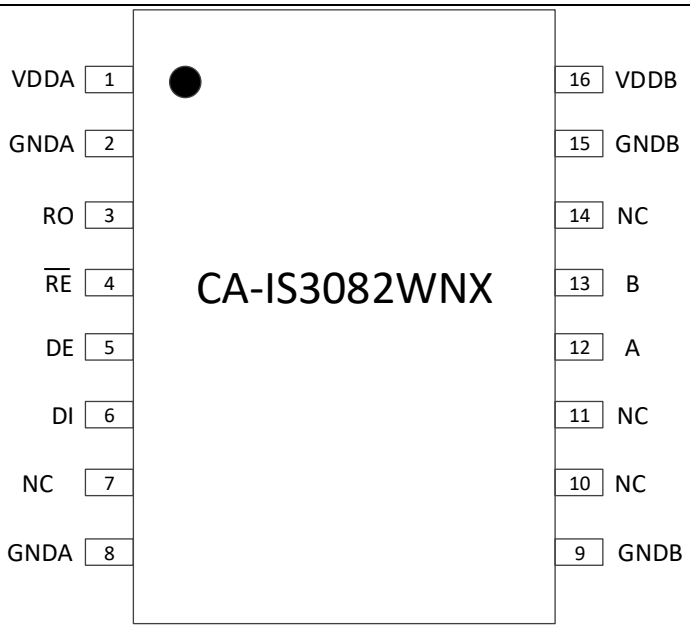


Figure 6-3. CA-IS3082WNX Top View

Table 6-3. CA-IS3082WNX Pin Description

Pin name	Pin number	Type	Description
VDDA	1	Power supply	Logic-Side Power Input. Bypass VDDA to GNDA with both 0.1μF and 1μF capacitors as close to the device as possible.
GNDA	2, 8	Ground	Logic-Side Ground. GNDA is the ground reference for digital signals.
RO	3	Digital I/O	Receiver Data Output. Drive $\overline{RE}$ low to enable receiver RX. With $\overline{RE}$ low, RO is high when (V_A –V_B) > -20mV and is low when (V_A – V_B) < -200mV.
$\overline{RE}$	4	Digital I/O	Receiver Output Enable. Driver $\overline{RE}$ low or connect to GNDA to enable RX. Drive $\overline{RE}$ high to disable RX.
DE	5	Digital I/O	Driver Output Enable. Drive DE high to enable bus driver outputs. Drive DE low or connect to GNDA to disable bus driver outputs. DE has an internal weak pull-down to GNDA.
DI	6	Digital I/O	Driver Input. With DE high, a logic low on DI forces the noninverting output (A) low and the inverting output (B) high; a logic high on DI forces the noninverting output high and the inverting output low.
NC	7	-	No internal connection
GNDB	9, 15	Ground	Cable Side Ground. GNDB is the ground reference for the RS-485/RS-422 bus signals.
NC	10, 11, 14	-	No internal connection
A	12	Bus I/O	Non-inverting RS-485/RS-422 receiver input and driver output.
B	13	Bus I/O	Inverting RS-485/RS-422 receiver input and driver output.
VDDB	16	Power supply	Cable Side Power Input. Bypass VDDB to GNDB with both 0.1μF and 1μF capacitor as close to the device as possible.

7. Specifications

7.1. Absolute Maximum Ratings[1]

Parameters		Minimum value	Maximum value	Unit
V_{DDA}, V_{DDB}	Power supply voltage[2]	-0.5	6.0	V
V_{IO}	Logic voltage (DI, DE, $\overline{RE}$, RO)	-0.5	V_{DDA}+0.5[3]	V
I_O	Output current on RO	-20	20	mA
T_J	Junction temperature		150	℃
T_{STG}	Storage temperature range	-65	150	℃

Notes:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. All voltage values except differential I/O bus voltages are with respect to the local ground (GNDA or GNDB) and are peak voltage values.
3. Maximum voltage must not be exceed 6V.

7.2. ESD Ratings

			Value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	Bus pin to GNDA	±4000	V
		Bus pin to GNDB	±8000	
		All other pins	±4000	
	Charged device model (CDM), per JEDEC Specification JESD22-C101, all pins[2]		±2000	

Notes:

1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
2. Per JEDEC document JEP157, 250V CDM allows safe manufacturing of standard ESD control process.

7.3. Recommended Operating Conditions

Parameters		Minimum value	Typical value	Maximum value	Unit
V_{DDA}	Power supply voltage on side A	2.375	3.3/5.0	5.5	V
V_{DDB}	Power supply voltage on side B(CA-IS3082/88)	3.0	3.3/5.0	5.5	V
V_{DDB}	Power supply voltage on side B(CA-IS3080/86)	3.0	5.0	5.5	V
V_{OC}	Common mode voltage at bus pins of the CA-IS3082/88: A, B	-7		12	V
V_{OC}	Common mode voltage at bus pins of the CA-IS3080/86: A, B, Y and Z	-15		15	V
V_{ID}	Differential input voltage V_{AB}	-12		12	V
V_{IH}	Input high voltage (RE, DI, DE to GNDA)	2.0			V
V_{IL}	Input low voltage (RE, DI, DE to GNDA)			0.8	V
DR	Data rate (CA-IS3080WX)			0.5	Mbps
DR	Data rate (CA-IS3082WX)			0.5	
DR	Data rate (CA-IS3082WNX)			0.5	
DR	Data rate (CA-IS3086WX)			10	
DR	Data rate (CA-IS3088WX)			10	
T_A	Environmental temperature	-40	27	125	℃

7.4. Thermal Information

Thermal Metric		CA-IS308x	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.4	℃/W

7.5. Insulation Specifications

Parameters		Test conditions	Specifications W	Unit
CLR	External Clearance[1]	Shortest terminal-to-terminal distance through air	8	mm
CPG	External Creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	32	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11)； IEC 60112	>600	V
	Material group	According to IEC 60664-1	I	
	IEC 60664-1 over-voltage category	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 400 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	
DIN V VDE V 0884-11:2017-01[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% product test)	7070	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[2]	Test method per IEC 60065, 1.2/50µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (production test)	6250	V_{PK}
q_{pd}	Apparent charge[3]	Method a, after input/output safety tests subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤5	
		Method b1, at routine test (100% production test) and preconditioning (sample test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤5	
C_{IO}	Barrier capacitance, input to output[4]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.5	pF
R_{IO}	Isolation resistance , input to output[4]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (certified) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	5000	V_{RMS}

Notes:

1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
2. Devices are immersed in oil during surge characterization.
3. The characterization charge is discharging charge (pd) caused by partial discharge.
4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together.

7.6. Safety-Related Certifications

VDE (pending)	UL	CQC	TUV
Certified according to DIN V VDE V 0884-11:2017-01	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-2011 and GB 8898-2011	Certified according to EN/IEC 61010-1:2010 (3rd Ed) and EN/IEC 62368-1:2014+A11:2017
	SOP16-W: 5000 V_{RMS}	Reinforced insulation 600 V_{RMS} Maximum working voltage (Altitude ≤ 5000 m)	5000 V_{RMS} reinforced insulation per EN/IEC 61010-1:2010 (3rd Ed) and EN/IEC 62368-1:2014+A11:2017, working voltage is up to 600 V_{RMS}
	Certificate number: E511334	Certificate number: CQC20001257126	CB certificate number: JPTUV-112094； DE 2-028138 AK certificate number: AK 50476734 0001； AK 50476735 0001

7.7. Electrical Characteristics

7.7.1. Driver

All typical specs are at V_{DDA} = 3.3V, V_{DDB} = 5V, T_A = 25°C,Min/Max specs are over recommended operating conditions unless otherwise specified.

CA-IS3082WX,CA-IS3088WX, CA-IS3082WNX

Parameters		Test conditions	Minimum value	TYP	Maximum value	Unit
$\|V_{OD1}\|$	Driver differential-output voltage	Open circuit voltage, unloaded bus.	2.7	4.6	5.5	V
$\|V_{OD2}\|$	Driver differential-output voltage	R_L = 54Ω, see Figure 8-1	1.5	3.2		V
$\Delta\|V_{OD}\|$	Change in differential output voltage between two states		-0.2		0.2	
V_{OC}	Common-mode output voltage		1	V_{DDB}/2	3	
ΔV_{OC}	change in steady-state common-mode output voltage between two states		-0.2		0.2	
I_{IL}	Input current	V_{DI}, V_{DE} = 0V or V_{DDA}	-20		20	μA
I_{os1}	Short-circuit output current (V_O = HIGH)	DE = $\overline{RE}$ = HIGH, DI = HIGH; V_Y = -7V, V_Z = 12V		90	150	mA
I_{os2}	Short-circuit output current (V_O = LOW)	DE = $\overline{RE}$ = HIGH, DI = LOW V_Y = 12V, V_Z = -7 V	-150	-90		mA
CMTI	Common mode transient immunity	V_{CM} = 1500V; see Figure 8-8	100	150		kV/μS
C_I	Input capacitance	VI = V_{DDA}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DDA} = 5 V		4		pF

CA-IS3080WX, CA-IS3086WX

Parameters		Test conditions	Minimum value	TYP	Maximum value	Unit
$\|V_{OD1}\|$	Driver differential-output voltage	Open circuit voltage, unloaded bus.	2.7	5	5.5	V
$\|V_{OD2}\|$	Driver differential-output voltage	R_L = 54Ω, see Figure 8-1	1.5	3.7		V
$\Delta\|V_{OD}\|$	Change in differential output voltage between two states		-0.2		0.2	
V_{OC}	Common-mode output voltage		1	V_{DDB}/2	3	
ΔV_{OC}	change in steady-state common-mode output voltage between two states		-0.2		0.2	
I_{IL}	Input current	V_{DI}, V_{DE} = 0V or V_{DDA}	-20		20	μA
I_{os1}	Short-circuit output current (V_O = HIGH)	DE = $\overline{RE}$ = HIGH, DI = HIGH; V_Y = -7V, V_Z = 12V	-250		250	mA
I_{os2}	Short-circuit output current (V_O = LOW)	DE = $\overline{RE}$ = HIGH, DI = LOW V_Y = 12V, V_Z = -7 V	-250		250	mA
CMTI	Common mode transient immunity	V_{CM} = 1500V; see Figure 8-8	100	150		kV/μS
C_I	Input capacitance	VI = V_{DDA}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DDA} = 5 V		4		pF

7.7.2. Receiver

All typical specs are at V_{DDA} = 3.3V, V_{DDB} = 5V, T_A = 25°C,Min/Max specs are over recommended operating conditions unless otherwise specified.

CA-IS3082WX,CA-IS3088WX, CA-IS3082WNX

Parameters		Test conditions	Minimum value	Typical value	Maximum value	Unit
V_{OH}	Output voltage high level	I_{OH} = -4mA;	V_{DDA}-0.4	4.8		V
V_{OL}	Output voltage low level	I_{OL} = 4mA;		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going input threshold voltage			-110	-50	mV
$V_{IT-(IN)}$	Negative-going input threshold voltage		-200	-140		mV
$V_{I(HYS)}$	Receiver input hysteresis			30		mV
I_I	Bus input current	V_A or V_B = 12 V, other logic input pins are connected to 0 V		70	600	µA
		V_A or V_B = 12 V, powered down, other logic input pins are connected to 0 V		70	300	
		V_A or V_B = –7 V, other logic input pins are connected to 0 V	–200	-40		
		V_A or V_B = –7 V, powered down, other logic input pins are connected to 0 V	–200	-40		
I_{IH}	Input current on the $\overline{RE}$ pin	V_{RE} = HIGH	–20		20	µA
I_{IL}	Input current on the $\overline{RE}$ pin	V_{RE} = LOW	–20		20	µA
R_{ID}	Differential input resistance	Measured between A and B	20			KΩ
C_D	Differential input capacitance	Input signal is f = 1.5 MHz, V_{pp} = 1V sinusoidal signals; measured between A and B		12		pF
C_I	Single-ended input capacitance	V_I = 0.4V × sin (2πft),f = 1MHz		18		pF

CA-IS3080WX, CA-IS3086WX

Parameters		Test conditions	Minimum value	Typical value	Maximum value	Unit
V_{OH}	Output voltage high level	I_{OH} = -4mA;	V_{DDA}-0.4	4.8		V
V_{OL}	Output voltage low level	I_{OL} = 4mA;		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going input threshold voltage			-100	-20	mV
$V_{IT-(IN)}$	Negative-going input threshold voltage		-200	-130		mV
$V_{I(HYS)}$	Receiver input hysteresis			30		mV
I_I	Bus input current	V_A or V_B = 12 V, other logic input pins are connected to 0 V		40	100	µA
		V_A or V_B = 12 V, powered down, other logic input pins are connected to 0 V		60	130	
		V_A or V_B = –7 V, other logic input pins are connected to 0 V	–100	–40		
		V_A or V_B = –7 V, powered down, other logic input pins are connected to 0 V	–100	–30		
I_{IH}	Input current on the $\overline{RE}$ pin	V_{RE} = HIGH	–20		20	µA
I_{IL}	Input current on the $\overline{RE}$ pin	V_{RE} = LOW	–20		20	µA
R_{ID}	Differential input resistance	Measured between A and B	96			KΩ
C_D	Differential input capacitance	Input signal is f = 1.5 MHz, V_{pp} = 1V sinusoidal signals; measured between A and B		17		pF
C_I	Single-ended input capacitance	V_I = 0.4 × sin (2πft), f = 1MHz		17		pF

7.8. Supply Current

All typical specs are at V_{DDA} = 3.3V, V_{DDB} = 5V, T_A = 25°C,Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameters		Test conditions		Minimum value	TYP	Maximum value	Unit
I_{CCA}	Logic side supply current	$\overline{RE}$ =0 or 1, DE=0 or 1	V_{DDA} = 3.3V			7.6	mA
		$\overline{RE}$ =0 or 1, DE =0 or 1	V_{DDA} = 5V			7.6	mA
I_{CCB}	Bus side supply current	$\overline{RE}$=0 or 1, DE =0, non-load				6.8	mA

7.9. Switching Characteristics

7.9.1. Driver

All typical specs are at V_{DDA} = 3.3V, V_{DDB} = 5V, T_A = 25°C,Min/Max specs are over recommended operating conditions unless otherwise specified.

CA-IS3082WX,CA-IS3088WX, CA-IS3082WNX

Parameters		Test conditions	Minimum value	Typical value	Maximum value	Unit
t_{PLH}, t_{PHL}	Driver Propagation Delay	see Figure 8-2 Figure 8-3 Figure 8-7 C_L=50pF		13	25	ns
PWD	Driver output skew $\lvert t_{PLH} - t_{PHL} \rvert$			3	12.5	ns
t_r	Differential output rise time			5	12	ns
t_f	Differential output fall time			5	12	ns
t_{PZH}/ t_{PZL}	Driver enable time, $\overline{RE}$ =0			15	35	ns
t_{PZH}/ t_{PZL}	Driver enable time, $\overline{RE}$ = V_{DDA}			6	12	µs
t_{PHZ}/ t_{PLZ}	Driver disable time			15	35	ns

CA-IS3080WX

Parameters		Test conditions	Minimum value	Typical value	Maximum value	Unit
t_{PLH}, t_{PHL}	Driver Propagation Delay	see Figure 8-2 Figure 8-3 Figure 8-7 C_L=50pF	200	300	620	ns
PWD	Driver output skew $\lvert t_{PLH} - t_{PHL} \rvert$			5	30	ns
t_r	Differential output rise time		250	360	680	ns
t_f	Differential output fall time		250	360	680	ns
t_{PZH}/ t_{PZL}	Driver enable time			7	10	µs
t_{PHZ}/ t_{PLZ}	Driver disable time			20	50	µs

CA-IS3086WX

Parameters		Test conditions	Minimum value	Typical value	Maximum value	Unit
t_{PLH}, t_{PHL}	Driver Propagation Delay	see Figure 8-2 Figure 8-3 Figure 8-7 C_L=50pF		16	48	ns
PWD	Driver output skew $\lvert t_{PLH} - t_{PHL} \rvert$			3	12.5	ns
t_r	Differential output rise time			3	10	ns
t_f	Differential output fall time			3	10	ns
t_{PZH}/ t_{PZL}	Driver enable time			24	90	ns
t_{PHZ}/ t_{PLZ}	Driver disable time			3	6	µs

7.9.2. Receiver

All typical specs are at V_{DDA} = 3.3V, V_{DDB} = 5V, T_A = 25°C,Min/Max specs are over recommended operating conditions unless otherwise specified.

CA-IS3082WX,CA-IS3088WX, CA-IS3082WNX

Parameters		Test conditions	Minimum value	Typical value	Maximum value	Unit
t_{PLH}, t_{PHL}	Receiver propagation delay	See Figure 8-4 Figure 8-5 Figure 8-6 C_L = 50pF		50	100	ns
PWD	Receiver output skew $\|t_{PLH} - t_{PHL}\|$				10	ns
t_r	Receiver output rise time			2.5	4	ns
t_f	Receiver output fall time			2.5	4	ns
t_{PHZ}/ t_{PLZ}	Receiver disable time			10	25	ns
t_{PZH}/ t_{PZL}	Receiver enable time, DE=V_{DDA}			40	90	ns
t_{PZH}/ t_{PZL}	Receiver enable time, DE=0V			6	12	µs

CA-IS3080WX

Parameters		Test conditions	Minimum value	Typical value	Maximum value	Unit
t_{PLH}, t_{PHL}	Receiver propagation delay	See Figure 8-4 Figure 8-5 Figure 8-6 C_L = 50pF		27	50	ns
PWD	Receiver output skew $\|t_{PLH} - t_{PHL}\|$			7	25	ns
t_r	Receiver output rise time			2.5	4	ns
t_f	Receiver output fall time			2.5	4	ns
t_{PHZ}/ t_{PLZ}	Receiver disable time			2	5	µs
t_{PZH}/ t_{PZL}	Receiver enable time			7	14	µs

CA-IS3086W

Parameters		Test conditions	Minimum value	Typical value	Maximum value	Unit
t_{PLH}, t_{PHL}	Receiver propagation delay	See Figure 8-4 Figure 8-5 Figure 8-6 C_L = 50pF		30	60	ns
PWD	Receiver output skew $\|t_{PLH} - t_{PHL}\|$			10	25	ns
t_r	Receiver output rise time			2.5	4	ns
t_f	Receiver output fall time			2.5	4	ns
t_{PHZ}/ t_{PLZ}	Receiver disable time			20	40	ns
t_{PZH}/ t_{PZL}	Receiver enable time			20	40	ns

8. Parameter Measurement Information

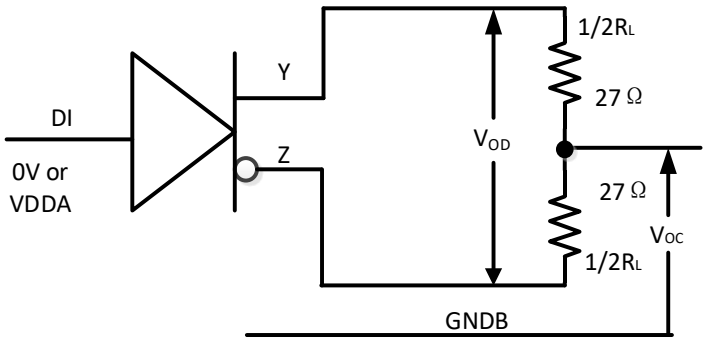
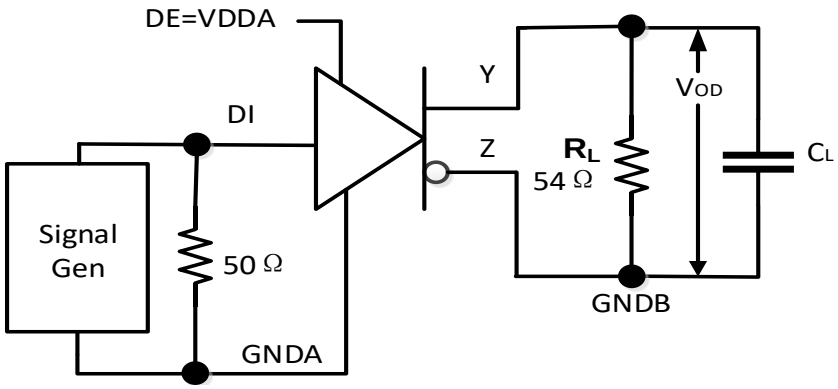


Figure 8-1. Driver DC test circuit



Notes:

1. 50Ω resister is only used for impedance matching.
2. C_L includes external circuit (fixture and instrumentation etc.) capacitance.

Figure 8-2. Driver transmission delay time test circuit

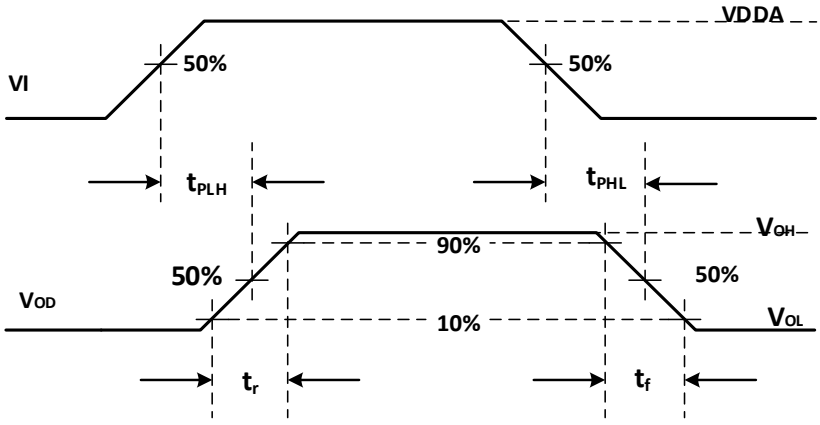
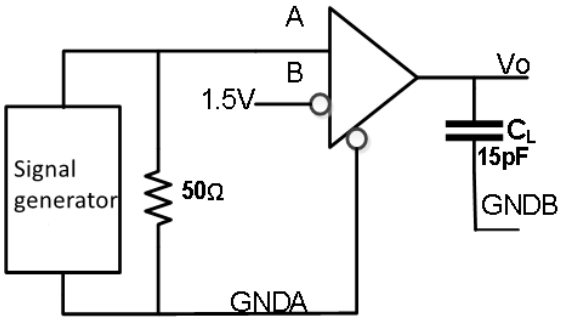


Figure 8-3. Driver propagation delays waveform



Notes:

1. 50Ω resister is only used for impedance matching.
2. C_L includes external circuit (fixture and instrumentation etc.) capacitance.

Figure 8-4. Receiver propagation delays test circuit

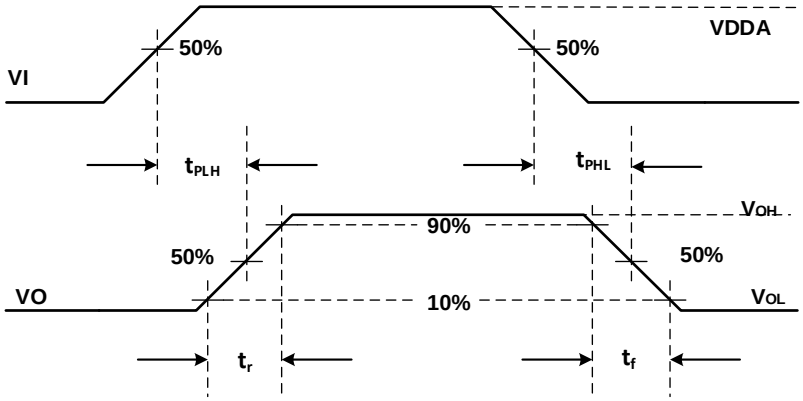


Figure 8-5. Receiver propagation delays waveform

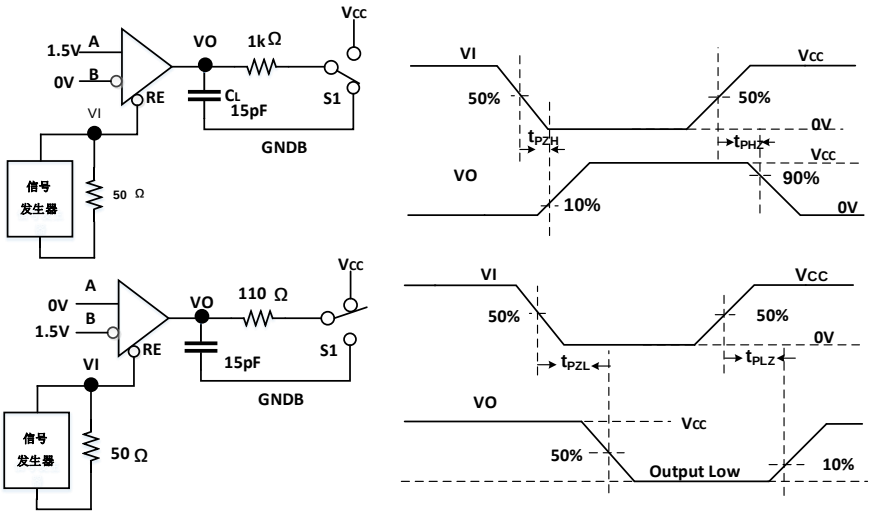
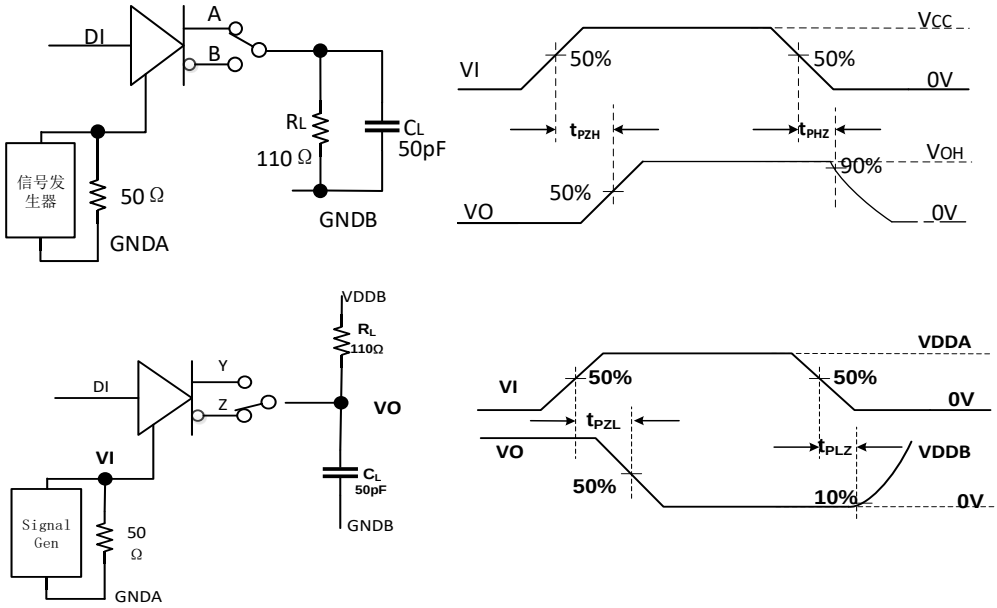


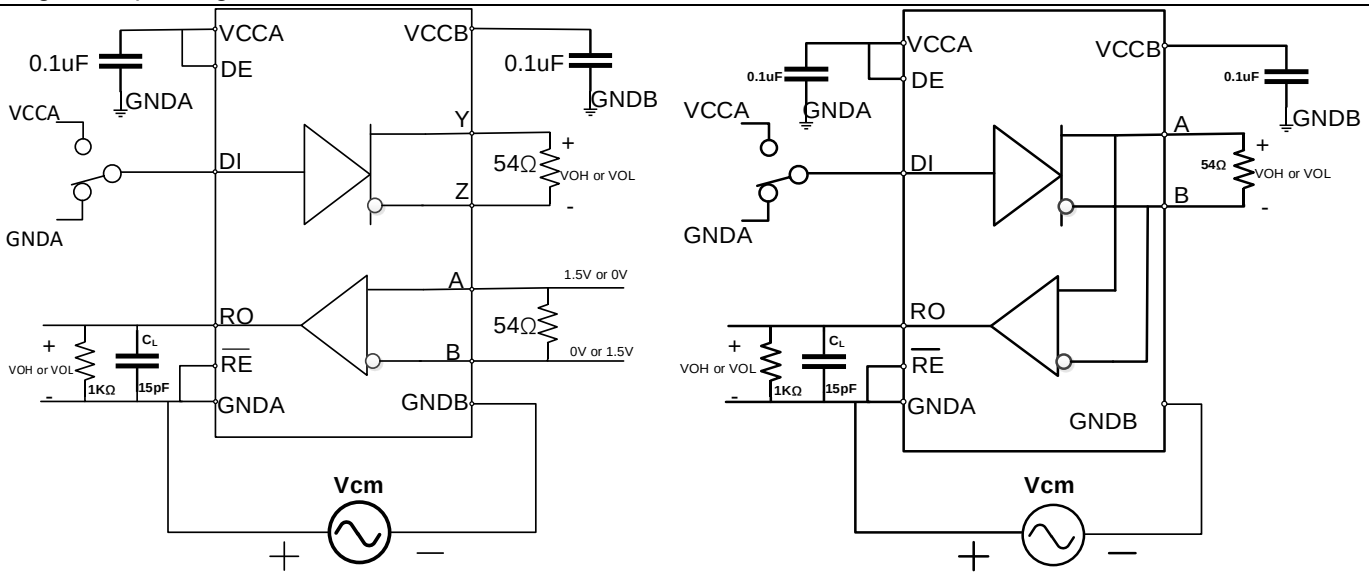
Figure 8-6. Receiver enable and disable function delay



Notes:

1. 50Ω resister is only used for impedance matching.
2. C_L includes external circuit (fixture and instrumentation etc.) capacitance.

Figure 8-7. Driver enable and disable function delay



Notes:

1. RL = 110 Ω for RS422, RL = 54 Ω for RS-485.
2. CL includes external circuit (fixture and instrumentation etc.) capacitance.

Figure 8-8. Common Mode Transient Immunity (CMTI) test for the full-duplex (left) and half-duplex (right)

9. Detailed Description

The CA-IS308x isolated RS485/RS422 transceivers provide up to 5kV$_{RMS}$ of galvanic isolation between the cable side (bus-side) of the transceiver and the controller side (logic-side). These devices feature up to 150 kV/μs common mode transient immunity, allow up to 10Mbps (CA-IS3086/88) or 0.5Mbps (CA-IS3080/82) communication across an isolation barrier. Robust isolation coupled with extended ESD protection and increased speed enables efficient communication in noisy environments, making them ideal for communication between logic-side and bus-side in a wide range of applications, such as motor drives, PLC communication modules, telecom rectifiers, elevators, HVACs etc. applications. Two mechanisms against excessive power dissipation caused by faults or bus contention. The first, a current limit on the driver output stage, provides immediate protection against short circuits over the entire common-mode voltage range. The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state. The CA-IS3080WX and CA-IS3086WX provide full-duplex transceivers, while the CA-IS3082WX, CA-IS3082WNX and CA-IS3088WX provide half-duplex transceivers for RS-485 communication.

9.1. Logic Input

The CA-IS308x devices include three digital inputs on the logic side: receiver enable, driver enable and driver digital input. The transmitter enable pin DE has an internal weak pull-down to GNDA； while the digital input DI and receiver enable $\overline{RE}$ pins have an internal pull-up to V_{DDA}. All devices use 1.5MΩ pull-up or pull-down resistor for the logic inputs, see Figure 9-1 for the inputs equivalent circuit.

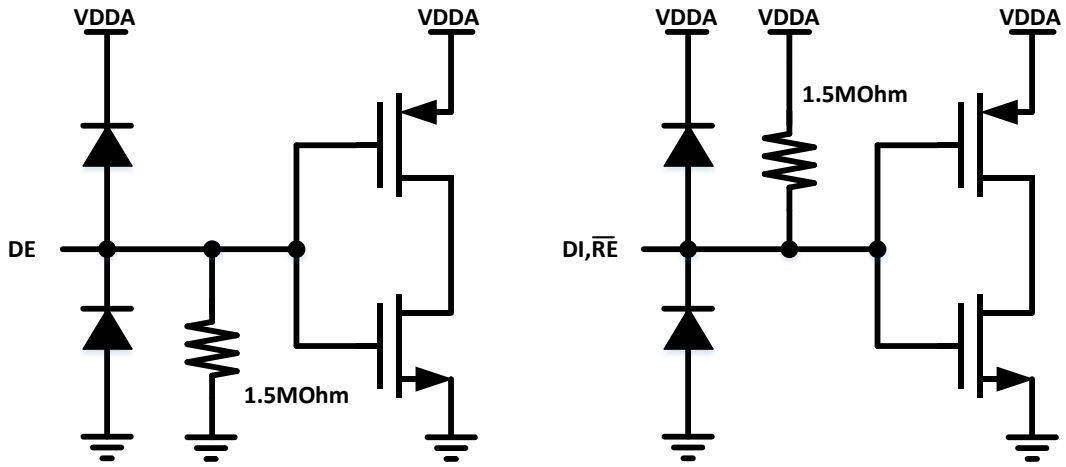


Figure 9-1. Input equivalent circuit

9.2. Fail-Safe Receiver

The receiver reads the differential input from the bus line (Y/A and Z/B) and transfers this data as a single-ended, logic-level output RO to the controller. Drive the enable input $\overline{RE}$ low to enable the receiver. Driver $\overline{RE}$ logic high to disable the receiver and put the receiver output RO in high impedance.

The CA-IS308x family of RS-485/RS-422 transceivers do not require fail-safe bias resistors because a true fail-safe feature is integrated into the devices. In true fail-safe, the receiver-threshold for logic-high and logic-low are $V_{IT+(IN)}$ and $V_{IT-(IN)}$, respectively. If the differential receiver input voltage of V_A-V_B is greater than or equal to $V_{IT+(IN)}$, RO is logic high when $\overline{RE}$ is low; RO is logic low when V_A-V_B is less than or equal to $V_{IT-(IN)}$ in case the receiver is enabled; thereby eliminating the need for fail-safe bias resistors while complying fully with the RS-485 standard, see Table 9-1 for the detail of receiver truth table. Fail-safe feature is used to keep the receiver's output in a defined state when the receiver is not connected to the cable, the cable has an open or the cable has a short.

Table 9-1. CA-IS308x Receiver Truth Table

VDDA	VDDB	DIFFERENTIAL INPUT	ENABLE	OUTPUT
		($V_A - V_B$)	($\overline{RE}$)	(RO)
Powered up	Powered up	$V_{IT+(IN)} \le V_A - V_B$	L	H
Powered up	Powered up	$V_{IT-(IN)} < V_A - V_B < V_{IT+(IN)}$	L	Indeterminate
Powered up	Powered up	$V_A - V_B \le V_{IT-(IN)}$	L	L
Powered up	Powered up	X	H	Hi-Z
Powered up	Powered up	X	open	Hi-Z
Powered up	Powered up	Open/Short/Idle	L	H
Powered down	Powered up	X	X	Hi-Z
Powered up	Powered down	X	L	H

Notes:

1. X = don't care; H = high level; L = low level; Hi-Z = high impedance.
2. $\overline{RE}$ has an internal weak pull-up to V_{DDA}.

9.3. Driver

The transmitter converts a single-ended input signal (DI) from the local controller to differential outputs for the bus lines Y/A and Z/B. The truth table for the transmitter is provided in Table 9-2. The driver outputs and receiver inputs are protected from ±8kV electrostatic discharge (ESD) to GNDB on the cable side, as specified by the Human Body Model (HBM). Also, the driver outputs feature short-circuit protection and thermal shutdown. The driver enable pin DE has an internal weak pull-down to GNDA. The driver input pin DI has an internal weak pull-up to $_{VDDA}$.

Table 9-2. CA-IS308x Transmitter Truth Table

VDDA	VDDB	INPUT	ENABLE INPUT	OUTPUTS	
		(DI)	(DE)	Y / A	Z / B
Powered up	Powered up	H	H	H	L
Powered up	Powered up	L	H	L	H
Powered up	Powered up	X	L	Hi-Z	Hi-Z
Powered up	Powered up	X	OPEN	Hi-Z	Hi-Z
Powered up	Powered up	OPEN	H	H	L
Powered down	Powered up	X	X	Hi-Z	Hi-Z
Powered up	Powered down	X	X	Hi-Z	Hi-Z
Powered down	Powered down	X	X	Hi-Z	Hi-Z

Notes:

1. X = don't care; H = high level; L = low level; Hi-Z = high impedance.
2. DE pin has an internal weak pull-down to GNDA. DI pin has an internal weak pull-up to V_{DDA}.

9.4. Protection Functions

9.4.1. Signal Isolation

The CA-IS308x devices integrated digital galvanic isolators using Chipanalog's capacitive isolation technology based on the ON-OFF keying (OOK) modulation scheme, allow data transmission between the controller side and cable side of the transceiver with different power domains.

9.4.2. Thermal Shutdown

If the junction temperature of the CA-IS308x device exceeds the thermal shutdown threshold $T_{J(shutdown)}$ (160°C, typ.), the driver outputs go high-impedance state. The shutdown condition is cleared when the junction temperature drops to normal operation temperature range of the device.

9.4.3. Current-Limit

The CA-IS308x protect the transmitter output stage against a short-circuit to a positive or negative voltage over the common mode voltage range (-7V to 12V for the CA-IS3082/88 and -15V to +15V for the CA-IS3080/86) by limiting the driver current. However, this will cause large supply current and dissipation. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit. The transmitter returns to normal operation once the short is removed.

10. Applications Information

The CA-IS308x family consists of half-duplex and full-duplex RS-485 transceivers commonly used for asynchronous data transmissions. For half-duplex devices, the driver and receiver enable pins allow for the configuration of different operating modes. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair.

10.1. Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. As seen in the following typical network application circuit, Figure 10-1 and Figure 10-2 show typical network application circuits for the full-duplex transceivers. Figure 10-1 is a bidirectional, full-duplex communication network, it includes a single driver on the master side and multiple receivers as slaves on one twisted pair; On another twisted pair cable, there are a single receiver on the master side and multiple drivers as slaves. Figure 10-2 is a point to pint communication network. Figure 10-3 shows typical network for the half-duplex transceivers, this reduces overall cabling requirements.

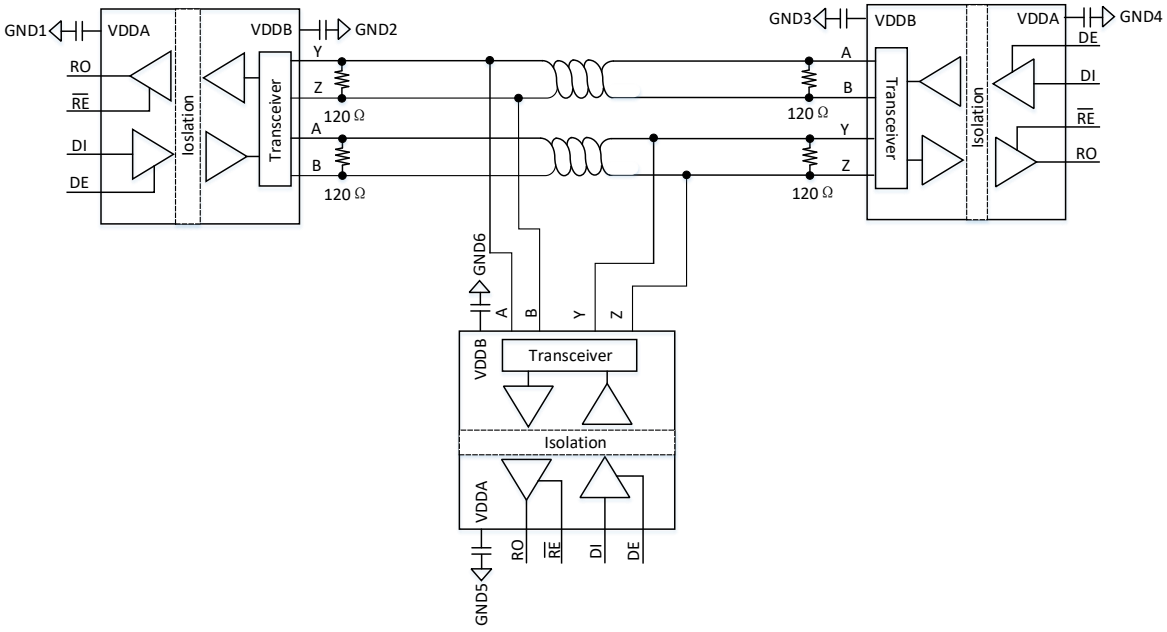


Figure 10-1. Typical isolated full-duple RS-422 application circuit

The maximum recommended data rate in the RS-485/RS422 network is 10Mbps, which can be achieved at a maximum cable length of 40ft (12m). The absolute maximum distance is 4000ft (1.2km) of cable, at which point, data rate is limited to 100kbps. These were the specifications made in the original standard, new RS-485 transceivers and cables are pushing the limit of RS-485 standard far beyond its original definitions. However, the maximum data rate is still limited by the bus loading, number of nodes, cable length etc. factors. For RS-485 network design, margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum data rate, number of nodes often lower. To minimize reflections, terminate the line at both ends with a termination resistor (120Ω in the typical application circuits), whose value matches the characteristic impedance (Z_0) of the cable, and keep stub lengths off the main line as short as possible. The termination resistors should always be placed at the far ends of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

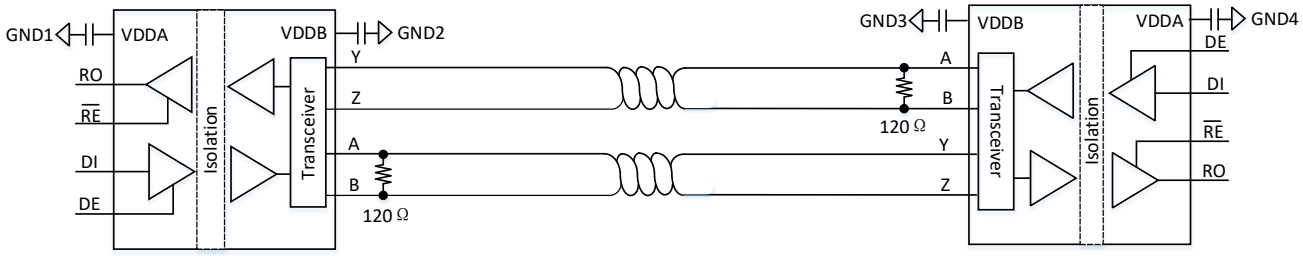


Figure 10-2. Typical isolated point to pint RS-485 network

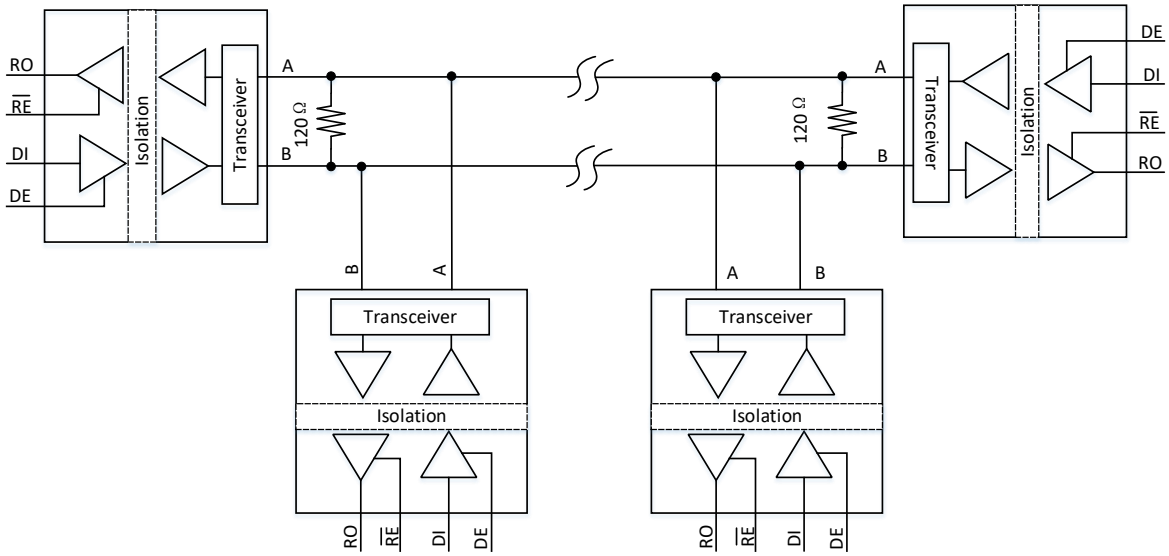


Figure 10-3. Typical isolated half-duplex RS-485 application circuit

10.2. Number of transceivers on the bus

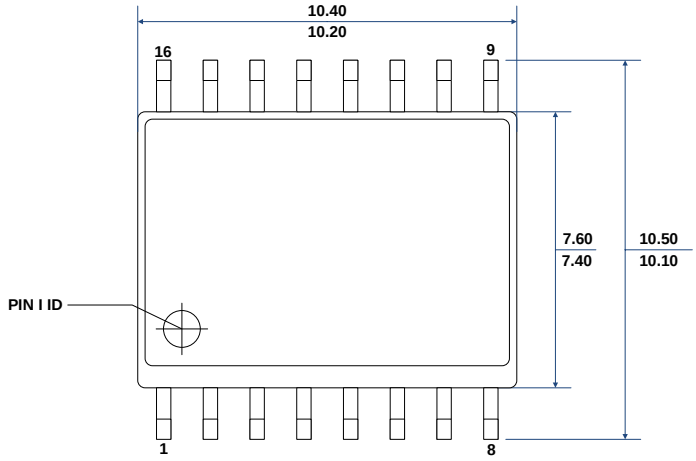
The maximum number of transceivers and receivers allowed depends on how much each device loads down the system. All devices connected to an RS-485 network should be characterized in regard to multiples or fractions of unit loads. The maximum number of unit loads allowed one twisted pair, assuming a properly terminated cable with a characteristic impedance of 120Ω or more, is 32 (375Ω). The CA-IS3080/86 transceivers have a 1/8-unit load (96kΩ) receiver, which allows up to 256 transceivers, connected in parallel, on one communication line. The receivers of CA-IS3082WX/CA-IS3082WNX and CA-IS3088WX feature 20kΩ input resistance, and allow up to 50 transceivers on the bus.

10.3. PCB Layout

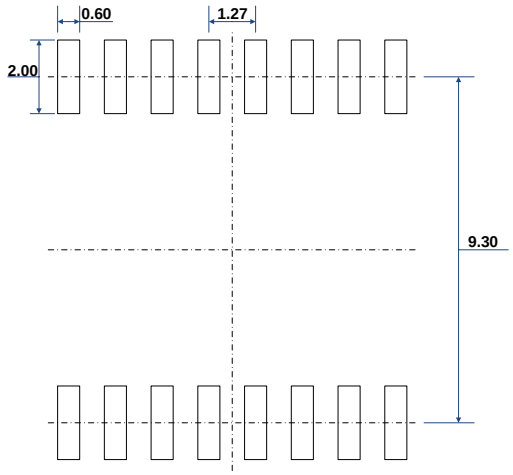
It is recommended to design an isolation channel underneath the isolator that is free from ground and signal planes. Any galvanic or metallic connection between the cable side and logic side will defeat the isolation. To make sure device operation is reliable at all data rates and supply voltages, the decoupling capacitors between VDDA and GNDA and between VDDB and GNDB are recommended. The capacitors should be located as close as possible to the IC to minimize inductance.

11. Package Information

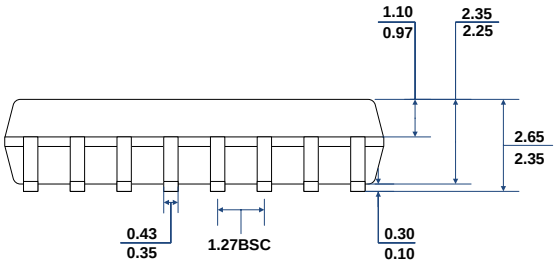
The following diagrams illustrate the dimension diagram of CA-IS308x series digital isolators packaged in SOIC16-WB wide package and the suggested pad dimension diagram, wherein dimensions are in millimeters.



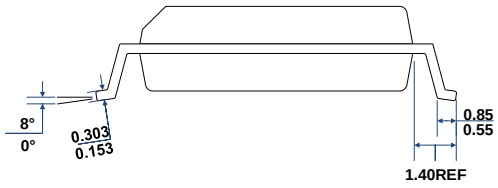
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT-SIDE VIEW

12. Soldering Temperature (reflow) Profile

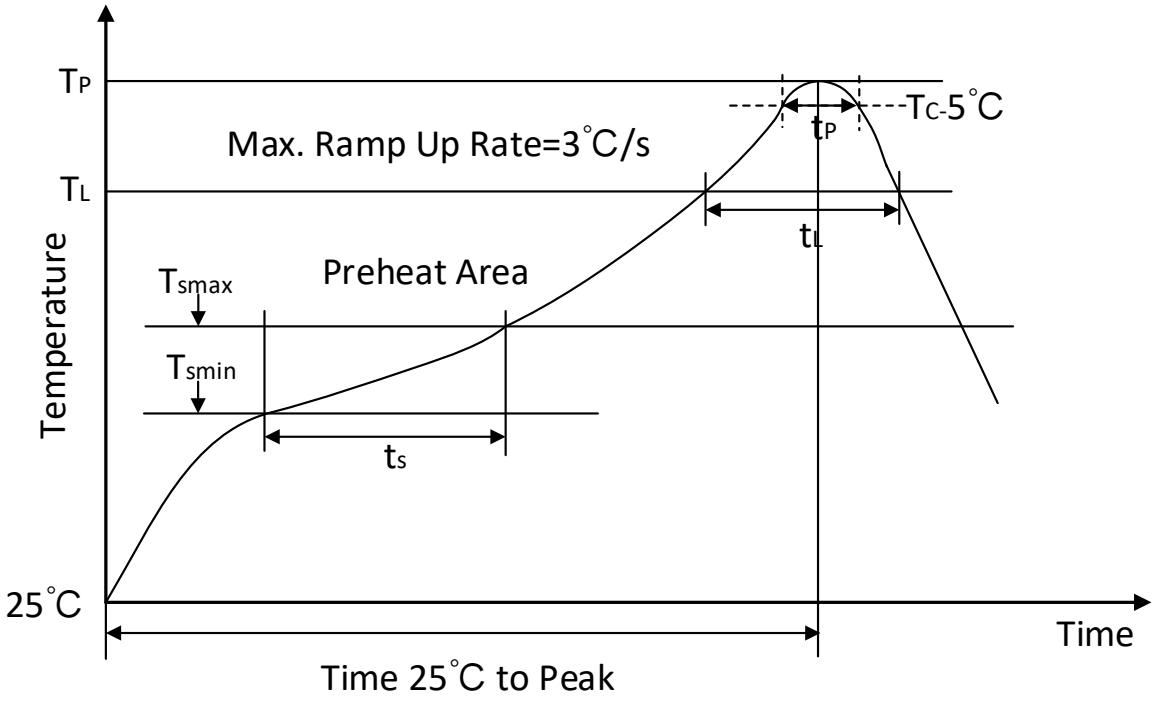


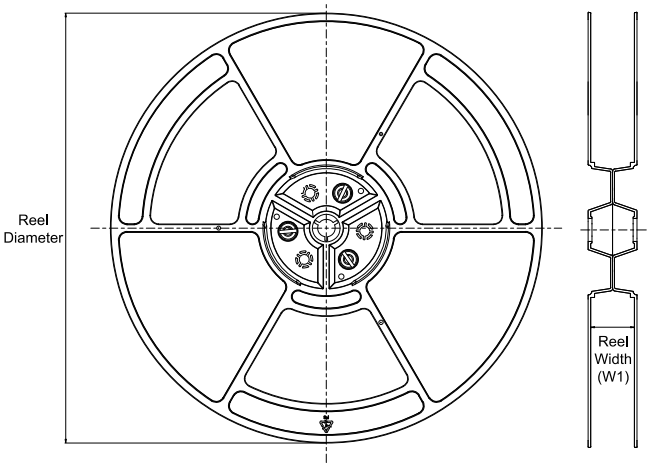
Figure 12-1. Soldering Temperature (reflow) Profile

Table 12-1. Soldering Temperature Parameter

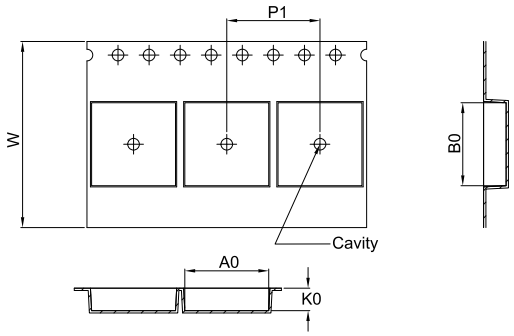
Profile Feature	Pb-Free Assembly
Average ramp-up rate(217 ℃ to Peak)	3℃/second max
Time of Preheat temp(from 150 ℃ to 200 ℃	60-120 second
Time to be maintained above 217 ℃	60-150 second
Peak temperature	260 +5/-0 ℃
Time within 5 ℃of actual peak temp	30 second
Ramp-down rate	6 ℃/second max.
Time from 25℃ to peak temp	8 minutes max

13. Tape and Reel Information

REEL DIMENSIONS

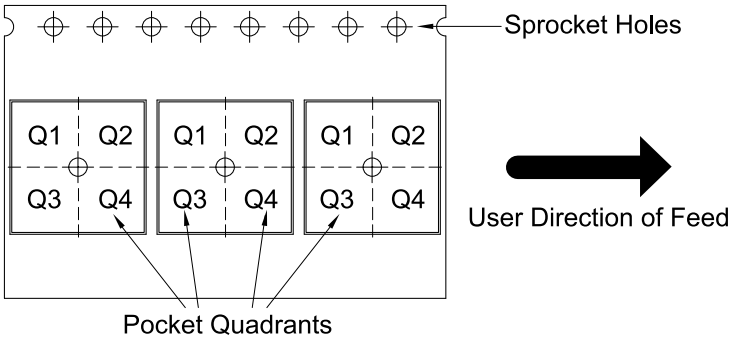


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Part #	Package	Package outline	# of pins	SPQ	Tape & Reel (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3080WX	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3086WX	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3082WX	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3082WNX	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3088WX	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1

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