High Voltage Half Bridge Gate Drive IC

General description

The ID7U603 is a high voltage, high speed power MOSFET and IGBT driver based on P_sub P_epi process. The floating channel driver can be used to drive two N-channel power MOSFETs or IGBTs in a half-bridge configuration which operates up to 600V. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications.

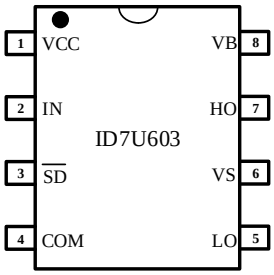
Features

- Operation to +600 V
- Typically 210 mA/360 mA Source/Sink current
- 5 V and 3.3 V input logic compatible
- dV/dt Immunity ±50 V/nsec
- Gate drive supply range from 10 V to 20 V
- UVLO for VCC and VBS
- Cross-conduction prevention logic with 520ns internal fixed Dead time
- Matched propagation delay for all channels

Application

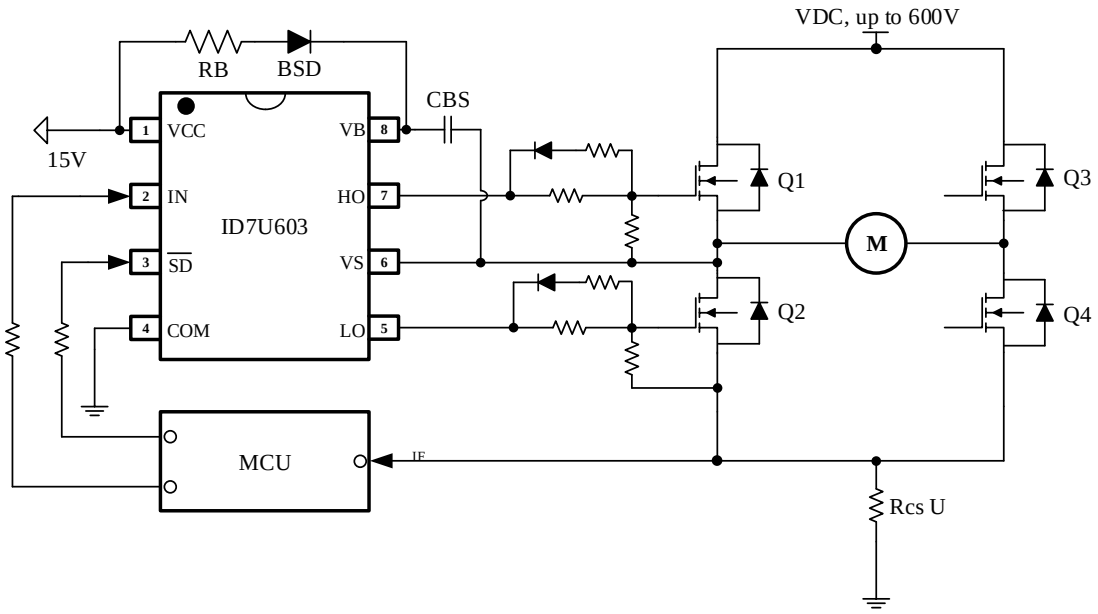
- Small and medium-power motor driver
- Power MOSFET or IGBT driver
- Lighting ballast
- Half-Bridge Power Converters
- Full-Bridge Power Converters

Package/Order Information



Order code	Package
ID7U603SEC-R1	SOP8

Typical Application Circuit



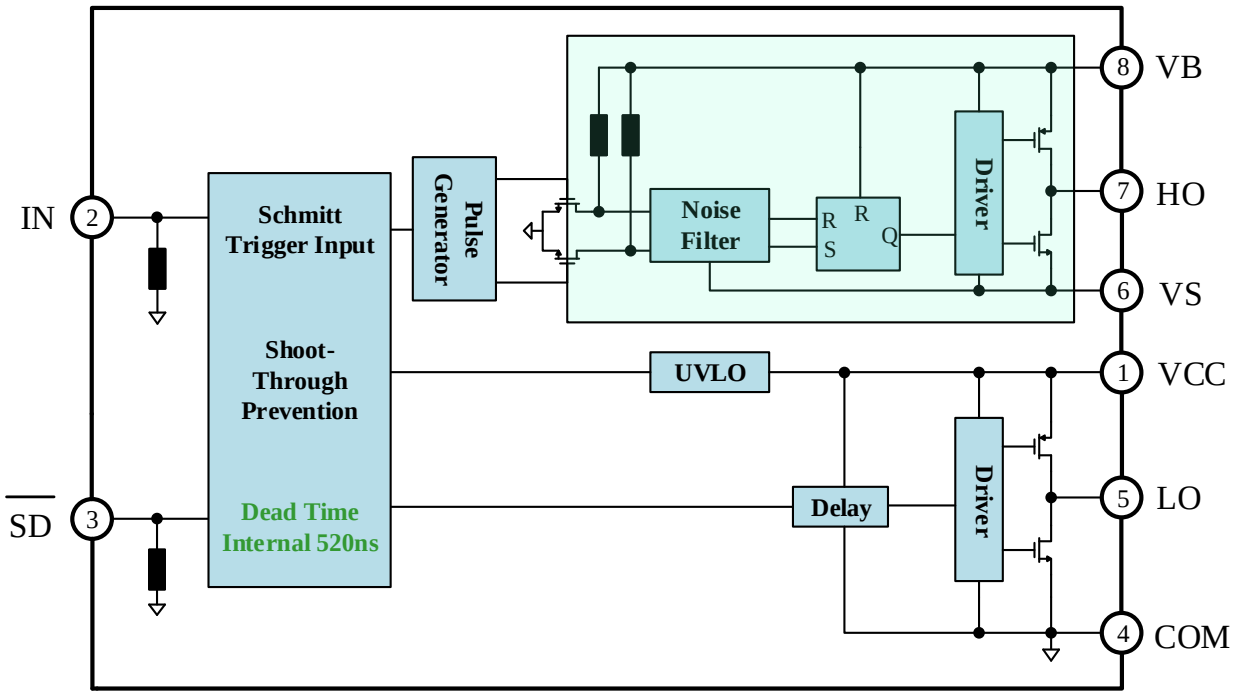
Note 1:

Add RB between V_{CC} and Bootstrap Diode, to avoid VB-VS over-shoot when CBS is charged first time. The recommended value for RB is 10 ohm.

Pin Definitions

Pin Name	Pin Number	Pin Function Description
VCC	1	Low side and main power supply
IN	2	Logic input for high and low side gate driver outputs (HO and LO)
$\overline{SD}$	3	Logic input for shutdown
COM	4	Low side return
LO	5	Low side gate drive output, Out phase with LIN
VS	6	High side floating supply return or bootstrap return
HO	7	High side gate drive output, in phase with HIN
VB	8	High side floating supply

Functional Block Diagram



Absolute Maximum Ratings

Exceeding these ratings may damage the device.
The absolute maximum ratings are stress ratings only at T_A=25℃, unless otherwise specified.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	-0.3	620	V
V_S	High side floating supply return	V_B - 20	V_B + 0.3	
V_{HO}	High side gate drive output	V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and main power supply	-0.3	20	
V_{LO}	Low side gate drive output	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input of IN and $\overline{SD}$	-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
ESD	HBM Model	2	—	kV
	Machine Model	200	—	V
P_D	Package Power Dissipation @ $T_A \leq 25°C$ (8 Lead SOP)	—	0.625	W
R_{thJA}	Thermal Resistance Junction to Ambient (8 Lead SOP)	—	200	℃ /W
T_J	Junction Temperature	—	150	℃
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply	V_S +10	V_S +20	V
V_S	High side floating supply return	-	600	
V_{HO}	High side gate drive output voltage	V_S	V_B	
V_{CC}	Low side supply	10	20	
V_{LO}	Low side gate drive output voltage	0	V_{CC}	
V_{IN}	Logic input voltage(IN & $\overline{SD}$)	0	V_{CC}	
T_A	Ambient temperature	-40	125	℃

Dynamic Electrical Characteristics

(V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25 ℃ unless otherwise specified.)

Symbol	Definition	MIN	TYP.	MAX.	Units
t_{on}	High side turn-on propagation delay	-	680	820	ns
t_{off}	High side turn-off propagation delay	-	150	220	
$t_{\overline{SD}}$	Low side turn-on propagation delay	-	160	220	
MT	Delay matching	-	-	60	
DT	Dead time	400	520	650	
t_r	Turn-on rise time	-	100	170	
t_f	Turn-off fall time	-	50	90	

Static Electrical Characteristics

(V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25 ℃ unless otherwise specified.)

Symbol	Definition	MIN.	TYP.	MAX.	Units
V_{IH}	Logic “1”(IN & $\overline{SD}$) input voltage	2.5	-	-	V
V_{IL}	Logic “0” (IN & $\overline{SD}$) input voltage	-	-	0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	-	-	0.3	
V_{OL}	Low level output voltage, V_O	-	-	0.3	
I_{QCC}	Quiescent V_{CC} supply current	-	150	270	uA
I_{QBS}	Quiescent V_B supply current	-	30	55	
I_{LK}	Leakage current from V_S(600V) to GND		-	10	
I_{IN+}	Logic “1” input bias current	-	6	10	
I_{IN-}	Logic “0” input bias current	-	-	1	
V_{CCU+}	V_{CC} supply UVLO threshold	-	8.9	-	V
V_{CCU-}		-	8.2	-	
I_{O+}	Output high short circuit pulsed current	130	210	-	mA
I_{O-}	Output low short circuit pulsed current	270	360	-	

Function Timing Diagram

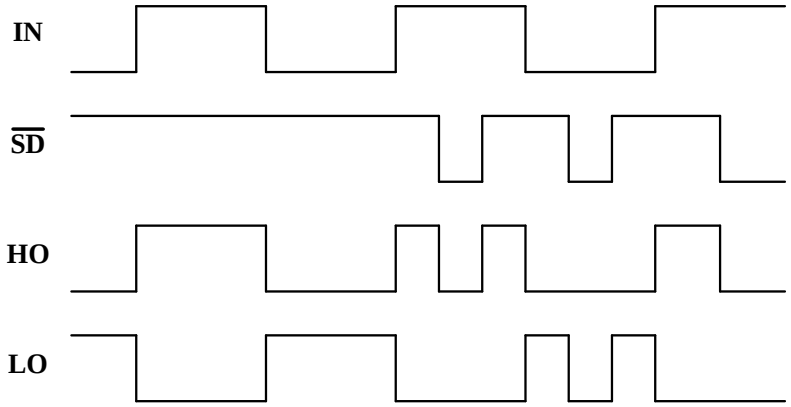


Fig.1 Input/output timing waveform

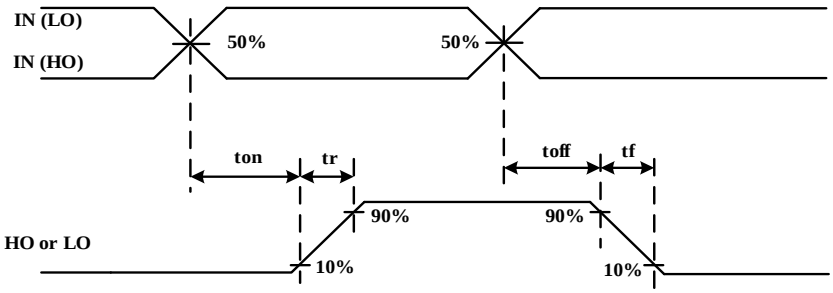


Fig.2 Switching time waveform definitions

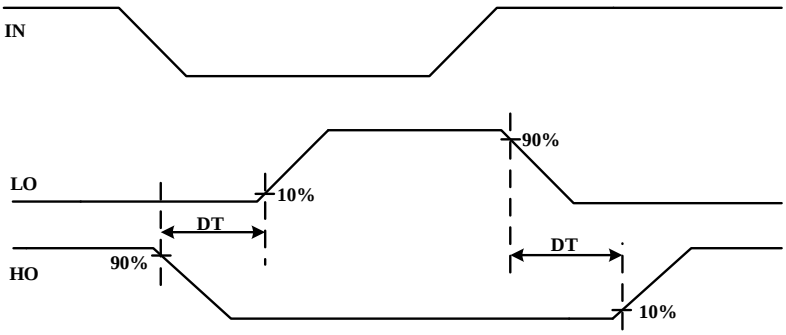
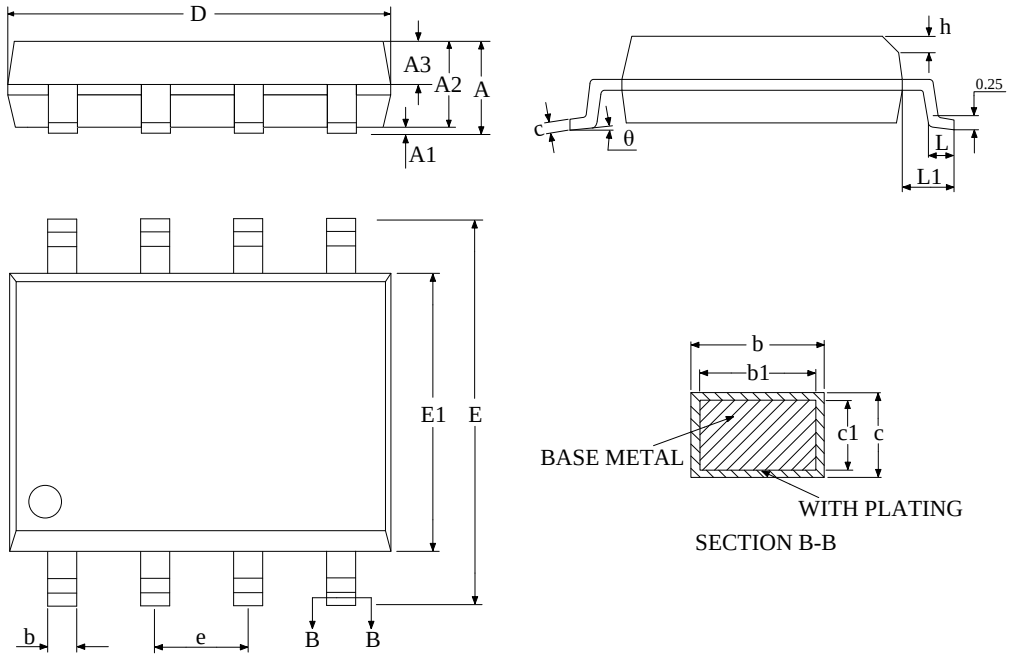


Fig.3 Dead-time waveform definitions

Package Information

Package Information SOP8



Size / Symbol	Min. (mm)	Max. (mm)	Size / Symbol	Min. (mm)	Max. (mm)
A	1.499	1.750	e	1.27TYP	
A1	0.102	0.249	h	-	-
A2	1.397	-	h1	0.254	0.457
b	0.406TYP		L	0.406	0.889
c	0.2TYP		θ1	12 °TYP	
D	4.852	4.952	θ2	12 °TYP	
E	5.842	6.198	θ3	0	8
E1	3.877	3.997	θ4	45	

Top mark	Package
iDR. ID7U603 YWWXXXXX	SOP8

Note：Y：Year Code；WW：Week Code；XXXXX：Internal Code

Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

Important Notice

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