AN5066
Application note

SRK1000/A/B adaptive synchronous rectification controller for flyback converters evaluation board family

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Introduction

The EVLSRK1000 in *Figure 1* is a family of demonstration boards intended for evaluation of the SRK1000 (SRK1000A and SRK1000B) controller in flyback converters with synchronous rectification (SR) at the transformer secondary side.

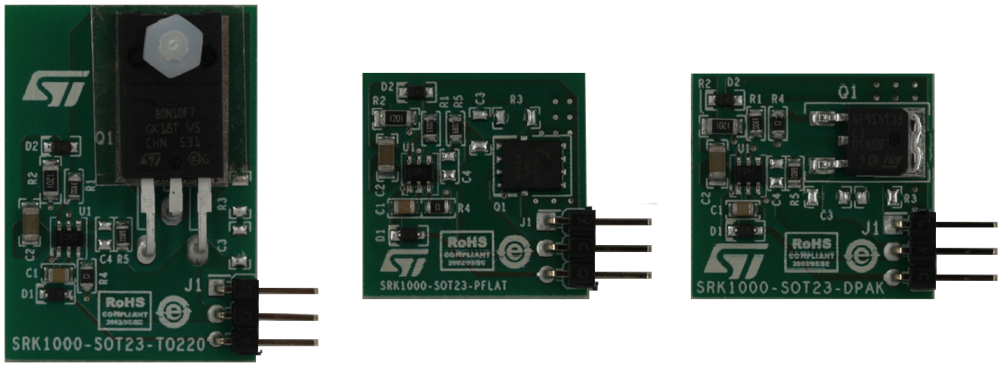
The first part of this application note is a description of the IC features, with some applicative information. Then the evaluation board schematic is described and the suggestion is provided on how to connect on an existing flyback converter. Finally, some consideration about circuit/layout optimization and thermal aspects are reported.

The PCB layout was realized in three different configurations, depending on the mounted SR MOSFET package. The various board codes are reported in *Table 1*.

Table 1. Demonstration board ordering codes

Ordering code	SR MOSFET P/N	MOSFET package	MOSFET V_{DSS} R_{DS_on}	Controller
EVLSRK1000-TO	STF80N10F7	TO220FP	100 V - 10 mΩ	SRK1000
EVLSRK1000-DP	STD80N10F7	DPAK	100 V - 10 mΩ	SRK1000
EVLSRK1000-PF	FDMS86103L	PowerFLAT 5x6	100 V - 8 mΩ	SRK1000
EVLSRK1000A-TO	STF80N10F7	TO220FP	100 V - 10 mΩ	SRK1000A
EVLSRK1000A-PF	FDMS86103L	PowerFLAT 5x6	100 V - 8 mΩ	SRK1000A
EVLSRK1000B-TO	STF80N10F7	TO220FP	100 V - 10 mΩ	SRK1000B
EVLSRK1000B-PF	FDMS86103L	PowerFLAT 5x6	100 V - 8 mΩ	SRK1000B

Figure 1. EVLSRK1000 - adaptive SR control for flyback converter



Contents

1 SRK1000 main characteristics

SRK1000 main features are described below. The values of the parameters mentioned in the following text are reported in the SRK1000 datasheet (see *1.*in *Section 5: References on page 26*). Please, refer to the datasheet also for a more detailed device operation description.

The SRK1000 SR controller implements a control scheme specific for secondary-side synchronous rectification in flyback converters, suitable for the operation in QR and mixed CCM/DCM. It provides a high current gate-drive output, capable of directly driving the N-channel power MOSFET.

This IC basically turns on the SR MOSFET as soon as it senses the current starts flowing through the body diode: triggered on the falling edge of the DVS signal decreasing below the cycle comparator threshold V_{TH_A}, the SRK1000 turns on the SR MOSFET, after a very short delay T_{D_On}. Then the controller turns off the SR MOSFET when the current approaches zero. There are two coexisting turn-off mechanisms (whichever triggers first), the first based on an adaptive algorithm, the second on the internal timer.

The adaptive turn-off consists of a ZCD_OFF comparator, where the DVS signal is compared to an adapting threshold, in such a way that, at the steady-state, the measured residual conduction time of the SR MOSFET body diode after the turn-off meets the target value T_{diode_off}.

In the steady-state, the internal timer basically turns off the SR MOSFET with a fixed anticipation time T_{ant_timer} with respect to the first rising edge of the DVS signal (above the V_{TH_A} threshold), basing on the duration of the previous switching period, in case of the fixed frequency CCM operation, or of the previous demagnetization time, in case of the QR operation.

The SRK1000 controller starts operation when the VCC pin voltage surpasses the turn-on threshold V_{CC_On}; then it stops operation when the V_{CC} voltage drops below the turn-off threshold V_{CC_Off}.

In order to guarantee SR switching even with low VCC supply voltage, in the case of chargers operating in CC regulation, the device is provided with the VAUX pin. When the VCC pin voltage decreases below the threshold $V_{CC\_SO\_On}$ (> V_{CC_Off}), an internal switch is turned on. This allows the capacitor on the VCC pin to be charged up to the turn-on threshold V_{CC_On} by a current drawn through the VAUX pin connected, for example, to the rectified SR MOSFET drain voltage or to another auxiliary voltage of the flyback transformer.

For the maximum flexibility in all kinds of applications and to overcome noise and ringing problems that may arise after the turn-on and turn-off events, the SRK1000 allows users to program the blanking time after the turn-on and provides three different values of the blanking time after the turn-off, according to the selected part number (SRK1000, SRK1000A, SRK1000B).

The device enters the low consumption mode when it detects the primary controller burst-mode operation or when the SR MOSFET conduction becomes lower than the programmed minimum TON. In this way, converter's efficiency improves at the light-load where synchronous rectification is no more beneficial.

After the converter restarts switching or the IC detects that the current conduction in the rectifiers has increased 20% above the min. TON programmed value, the IC exits the low consumption mode and resumes the switching operation.

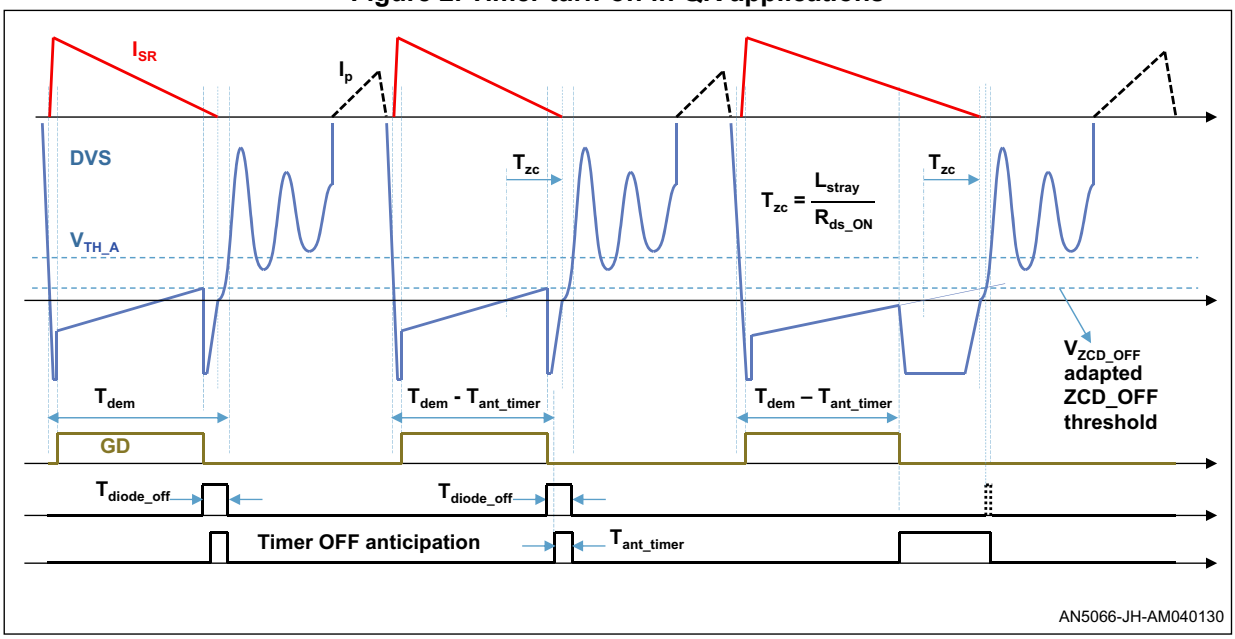
1.1 QR and FF operation

As already mentioned above, the controller can operate both in quasi-resonant applications and in fixed frequency (FF) mixed DCM-CCM applications. For each of these two operating modes, the SRK1000 internal timer needs to be set in a different way for a correct operation. On this purpose, the user can select the proper timer mode by means of an external capacitor on the TON pin, whose presence is detected during the pinstrap phase at the device start-up:

- For QR operation no capacitor mounted on TON pin
- For FF mixed DCM-CCM operation 100 pF capacitor mounted on TON pin

The timer operation in QR applications is set in such a way that in the current cycle it provides a turn-off with anticipation T_{ant_timer} with respect to the duration of the demagnetization time in the previous cycle. This is illustrated in *Figure 2*.

Figure 2. Timer turn-off in QR applications

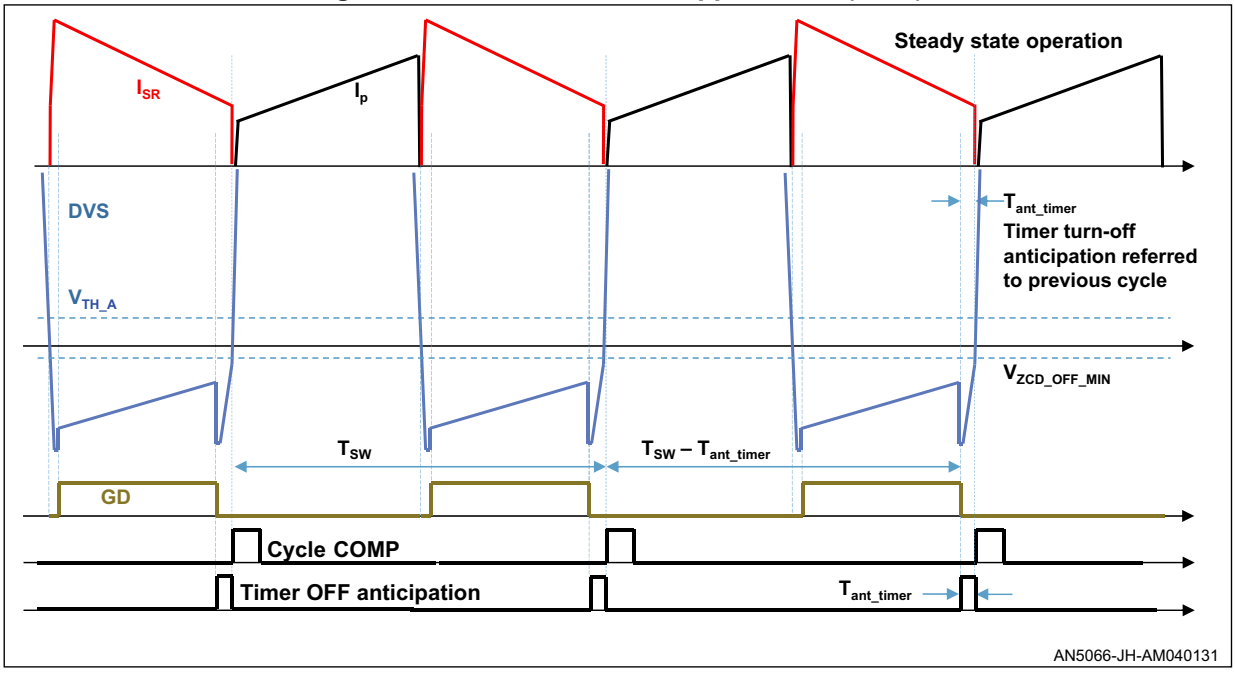


Suppose the circuit is in steady-state condition and the adaptive threshold of the ZCD comparator is adapted (i.e. the residual conduction of the body diode is T_{diode_off}, while the ZCD comparator accomplishes the turn-off). In this condition, also the timer is ready for the turn-off: if T_{dem} is the steady-state demagnetization time in the cycle on the left of *Figure 2*, in the subsequent cycle the timer would turn off with a delay of T_{dem} - T_{ant_timer} from the DVS signal falling below V_{TH_A}. Of course, in this steady-state condition the ZCD turn-off always anticipates the timer turn-off, (since it is always verified $T_{diode\_off} > T_{ant\_timer}$). If a low-to-high load transition happens and the demagnetization time increases (due to a sudden output voltage decrease) like in the last cycle of *Figure 2*, the ZCD turn-off would be too late (since the ZCD adapted threshold stays unchanged): in this case, the timer will accomplish the turn-off, avoiding an undesired current inversion.

During fixed frequency mixed CCM-DCM operation, the timer is set in such a way that in the current cycle it provides a turn-off with an anticipation T_{ant_timer} with respect to the duration of the complete switching period detected in previous cycles. This is illustrated in *Figure 3* and *Figure 4*, for CCM and DCM respectively: in both cases the switching period start is detected at the first rising edge of the DVS signal above the V_{TH_A} threshold by the cycle

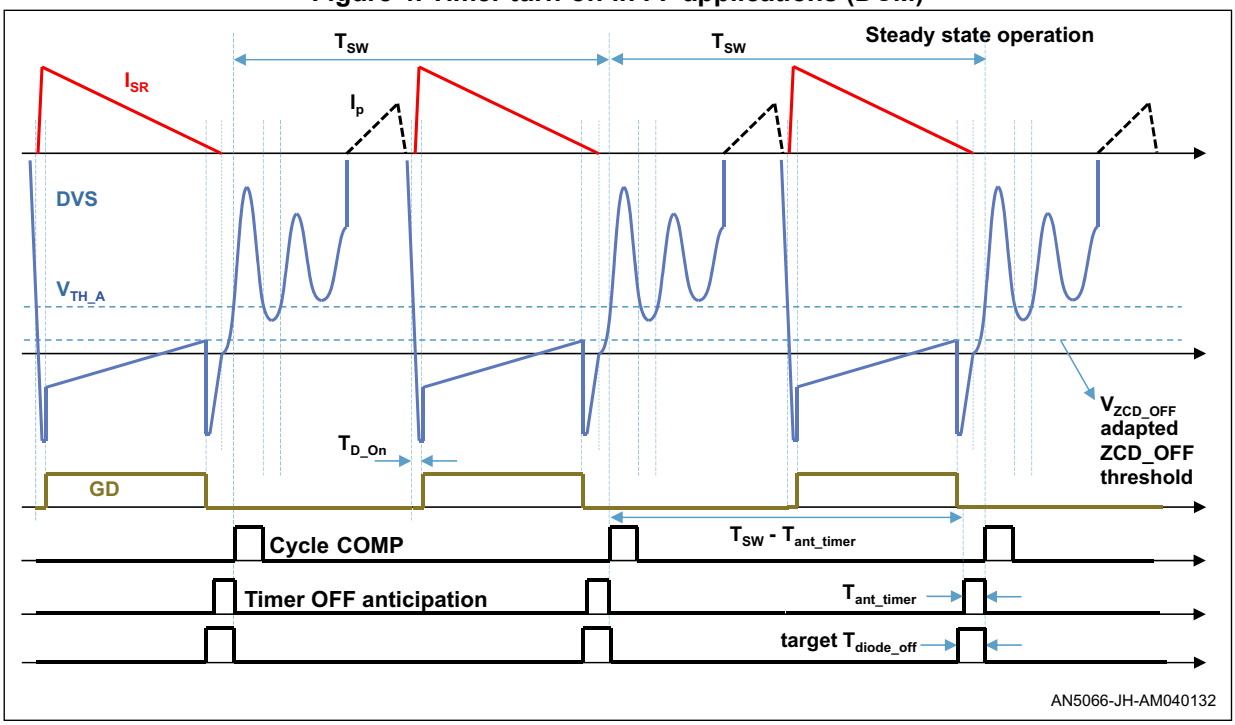
comparator (in the DCM case, the ringing after demagnetization is filtered by the blanking time after turn-off).

Figure 3. Timer turn-off in FF applications (CCM)



In full CCM steady-state operation, the timer accomplishes the turn-off always: in fact in this condition the adaptive comparator cannot trigger, since the DVS signal is always lower than the $V_{ZCD\_OFF\_MIN}$, minimum (adapting) threshold of the comparator.

Figure 4. Timer turn-off in FF applications (DCM)

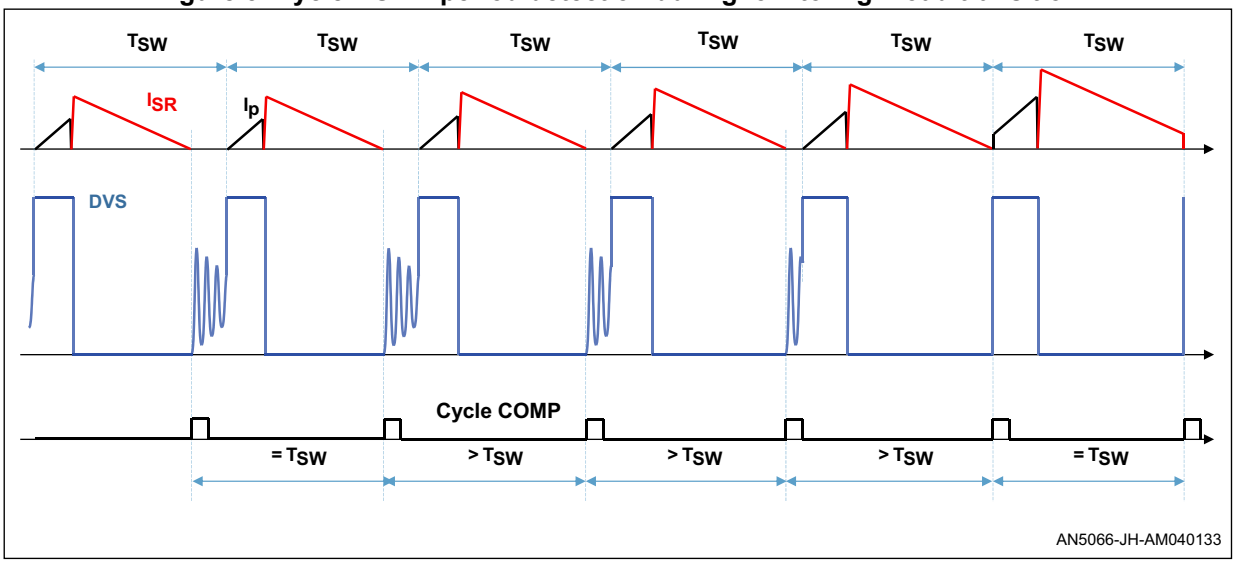


In fixed frequency DCM steady-state, instead, the adaptive ZCD comparator triggers the turn-off so that the target residual conduction T_{diode_off} of the body diode is met, while the timer cannot turn off, since the target T_{diode_off} is longer than the anticipation time T_{ant_timer} (like in the QR operation case).

There is a range of load where the circuit still operates in CCM but is rather close to DCM, and the DVS signal can reach the minimum ZCD comparator threshold $V_{ZCD\_OFF\_MIN}$: in this load range, there is some interaction between the timer turn-off and adaptive turn-off.

During a load transition low-to-high, where the operation passes from DCM to CCM, the switching period detected by the cycle comparator increases from the current to the next cycle (though the real switching frequency set by the primary controller remains absolutely constant). This happens because (refer to *Figure 5*) the high-impedance period (during the ringing after demagnetization) progressively decreases, while the demagnetization time increases (due to the higher energy request consequent to load increase). Now, if the period is sensed increasing cycle by cycle, the timer should update accordingly. After some cycles, however, the transition ends and the sensed period suddenly reduces to the real switching period: therefore, a current inversion would present in case the timer had been updated progressively cycle by cycle. In this phase, also the ZCD comparator is adapting the threshold from the level proper to the DCM operation to the one relative to CCM and, therefore, would not be in time to turn off.

Figure 5. Cycle COMP period detection during low-to-high load transition



Hence, to avoid current inversions in these transitions, the SRK1000 does not update the timer cycle by cycle but only once every 4 cycles that a period increase is detected; in addition, the turn-off delay increase in the fourth cycle is limited to maximum T_{timer_step}.

There is an impact of the above described slow adapting of the timer in applications where the switching frequency is modulated for the EMI reduction. In fact, during the time interval where the modulated switching period increases, the timer update is limited to maximum T_{timer_step} every 4 cycles. Therefore, the maximum switching period increase from the current to the next cycle has to be lower than $T_{timer\_step}/4$ otherwise the timer turn-off will be progressively anticipated and body diode conduction will increase.

In the time interval during which the switching period goes decreasing (along the modulating frequency cycle), the SRK1000 timer update is not limited like in the previous time interval.

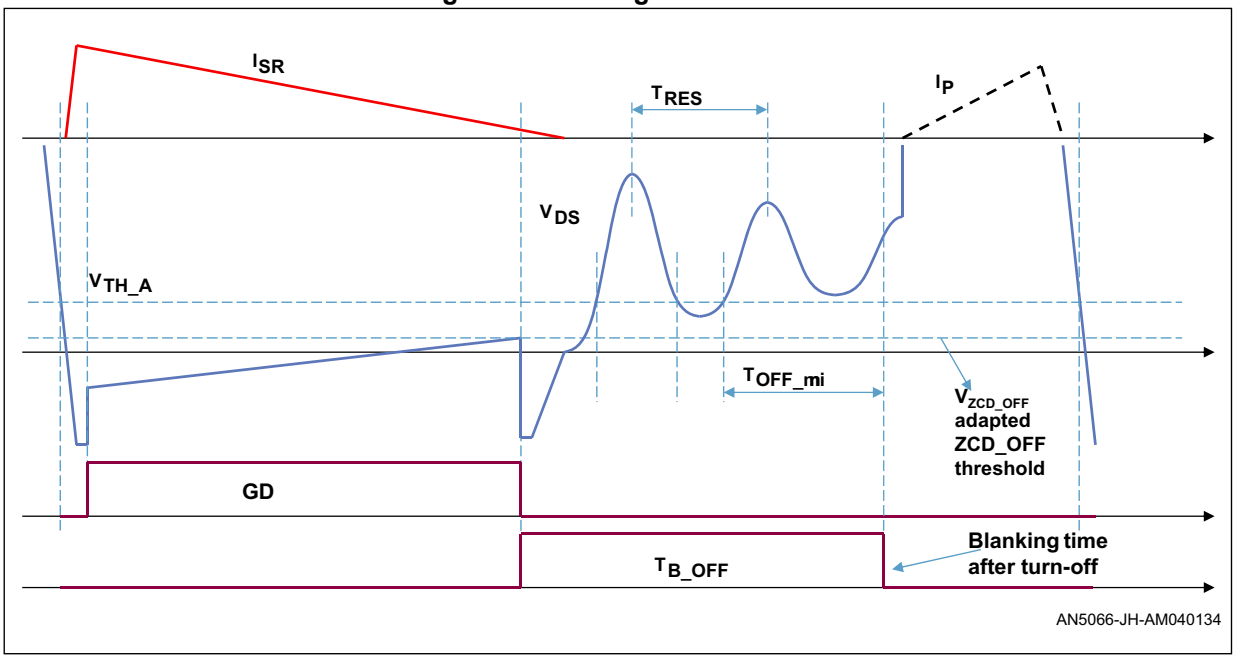
The only requirement is that the period decrease from the current to the next cycle has to be lower than T_{ant_timer}, otherwise a current inversion will occur.

1.2 Device selection for blanking after turn-off

The device is provided with three different values of blanking after the turn-off (T_{OFF_min}), according to the selected option (SRK1000, SRK1000A and SRK1000B). The aim of the blanking time is to filter the ringing after transformer demagnetization, present on the DVS signal, both in QR applications and in FF applications during the DCM operation and that, otherwise, could trigger an undue turn-on if the ringing voltage should decrease below the V_{TH_A} threshold.

The blanking time filtering effect is illustrated in *Figure 6*, where the dumped ringing after demagnetization can cross the V_{TH_A} threshold.

Figure 6. Blanking after turn-off



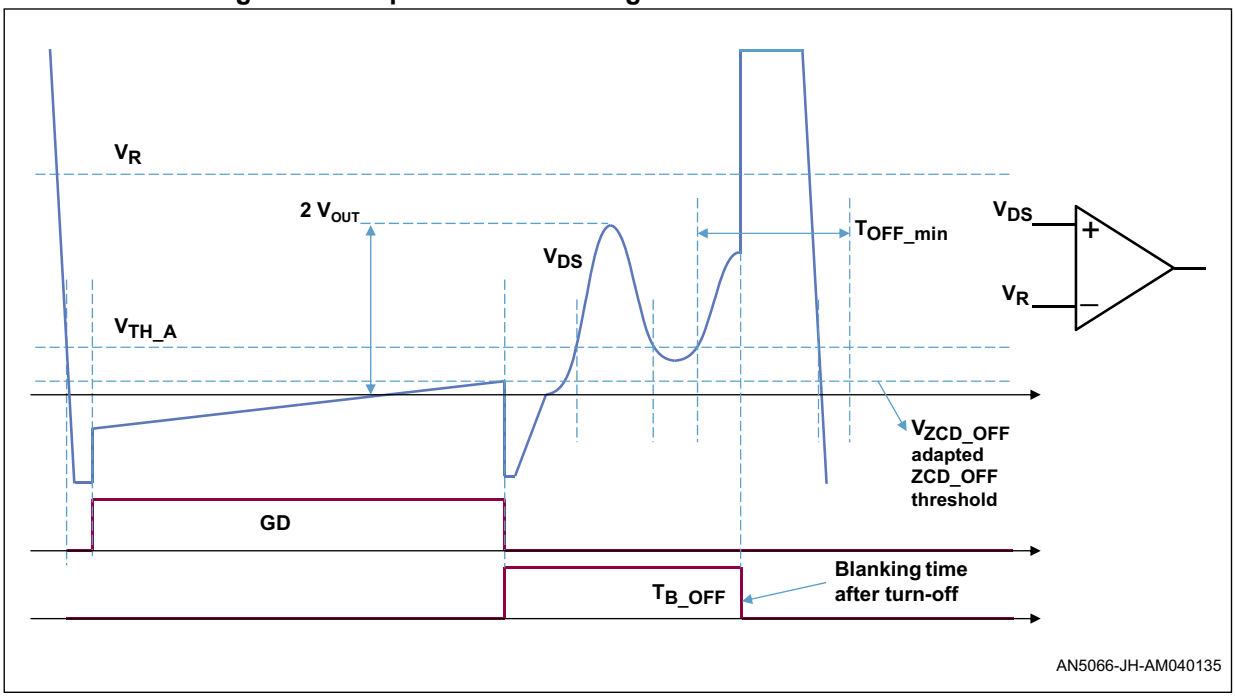
The internally fixed T_{OFF_min} of the device provides a total blanking time from the turn-off to the time instant occurring after the DVS ringing voltage stays permanently higher than V_{TH_A} for T_{OFF_MIN}. Therefore, the user has to select the device with $T_{OFF\_min} > T_{RES}$ (the ringing period).

In some operating conditions (at the reduced load and high input voltage, where the primary switch ON time T_{p_ON} is short), it may happen that the chosen T_{OFF_min} results longer than $T_{RES}/2+T_{p\_ON}$. In this case, the total blanking would filter also the DVS falling edge at beginning of SR MOSFET conduction, with a consequent skipping of the driving cycle. To avoid this, the IC is provided with an internal comparator referenced to a voltage $V_R = 2.83 \cdot V_{out}$ and sensing the DVS signal (really, the V_R and DVS signal are conveniently scaled at comparator inputs by resistive dividers). Referring to *Figure 7*, when the DVS signal surpasses the threshold V_R, the blanking time after the turn-off is terminated (independently from T_{OFF_min}). Of course, for the correct operation of the comparator, the V_{out} voltage information has to be available on the VCC pin (or V_{out} - V_F, in case VAUX

functionality is used and a decoupling Schottky diode is necessary from V_{out} to the VCC pin). This means that the IC needs to be supplied by the V_{out}.

The ringing after demagnetization on the DVS signal is dumped through the transformer ac resistance; therefore, if this ringing never crosses V_{TH_A}, the device with the shortest T_{OFF_min} can be selected and in this case, the internal comparator referenced to V_R for the blanking termination would not be necessary at all (since T_{OFF_min} blanking will terminate in advance).

Figure 7. Comparator for blanking time after turn-off termination

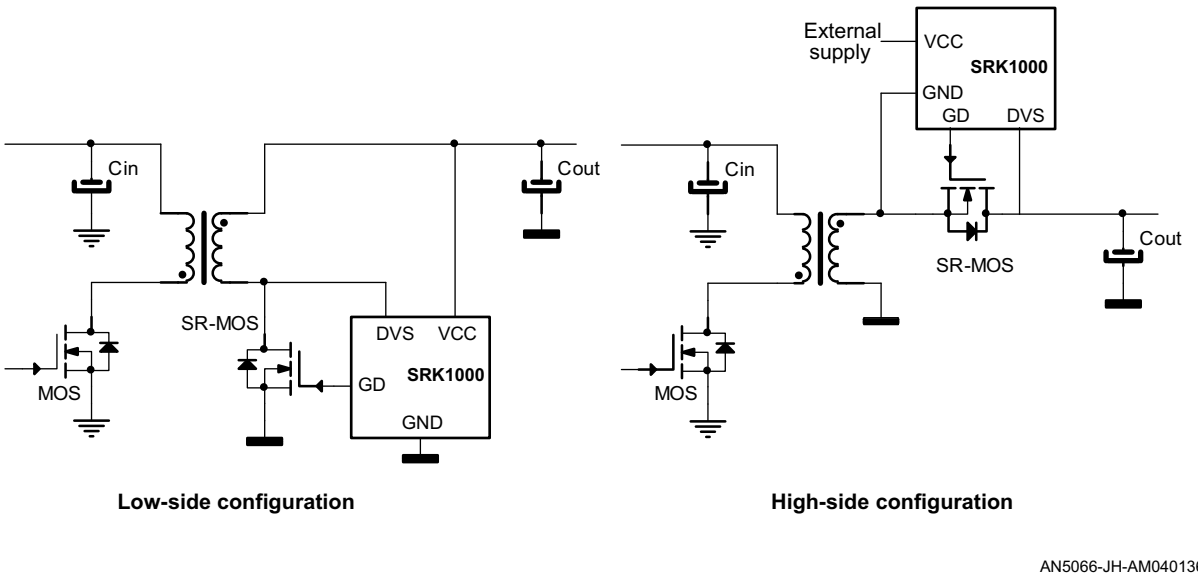


1.3 Low-side and high-side configuration

Normally the device has to be intended for applications where the SR MOSFET is mounted with the source terminal connected to secondary GND (the so called “low-side configuration”), that allows to directly supply the VCC pin through the output voltage of the circuit (necessary for the reasons detailed above).

In applications where the dumping effect of the transformer is such that the ringing voltage after demagnetization presents valley voltage that never crosses $V_{TH\_A,}$ the SRK1000 with the lowest T_{OFF_min} can be used, in which case also the “high-side configuration” can be implemented. *Figure 8* shows the basic scheme of the low-side and high-side configuration.

Figure 8. Low-side and high-side configuration



For the high-side configuration, an external supply is necessary for the VCC pin of the SRK1000. This could be derived, for example, through a further auxiliary winding of the transformer at the secondary side, added on the top of the winding used for the output voltage. Alternatively to this method, a charge pump can be implemented, based on the rectification of the switching waveform across the SR MOSFET drain-source.

Please, refer to *Section : How to implement the board in the converter on page 16* for further details on configurations.

1.4 TON pin programming usage

TON pin programming relates to several design aspects of the application:

1. **Filtering**: first of all, the TON pin is used to filter the noise arising after the SR MOSFET turn-on, by programming a blanking time [refer to “Minimum TON programming” paragraph, in the SRK1000 datasheet (see *1.*in *Section 5: References on page 26*)] that prevents a premature turn-off. This noise mainly depends on the driver current path layout and on transformer leakage inductance.

   If the driver current path is carefully layouted (reducing its stray inductance and loop area) the required blanking time can be shorter; the same happens also if the transformer leakage inductance effect is minimized by a proper transformer construction and/or by the usage of a clamp circuit across the transformer primary winding. Generally, a R2CD clamp is more effective than a standard RCD clamp in these kinds of applications, since it dumps very quickly the ringing after leakage demagnetization, leading also to a reduction of EMI noise.

2. **Sleep-mode:** furthermore, the TON pin allows to the user to program a minimum turn-on time to enter the sleep-mode when the load is progressively reduced to a level where the synchronous rectification is not any longer beneficial in the specific application [refer to “Low consumption mode operation: sleep-mode and burst-mode” paragraph in SRK1000 datasheet (see *1.*in *Section 5: References*)]. In case the user prefers the usage of the burst-mode operation of the flyback controller when in light-load conditions, the minimum TON can be programmed to be always lower than the level where the system enters the burst-mode.

3. **Adaptive gate-drive:** finally, the TON programming helps reducing driving losses at reduced loads (with consequent efficiency optimization) by modulating the driver voltage high-level [refer to “Adaptive gate-drive” paragraph in the SRK1000 datasheet (see *1.*in *Section 5: References on page 26*)].

   This optimization can be done in the following way:

   a) Select the minimum resistor $R_{TON.min}$ that provides a blanking time suitable to avoid a premature turn-off (in all line and load conditions).

   b) Check which is the minimum transformer demagnetization time while reducing the load, just before entering the burst-mode operation of the primary controller (should be checked both at minimum and at maximum input voltage).

   c) Select the maximum resistor $R_{TON.max}$ that assures the SRK1000 never enters the automatic sleep-mode before the primary burst-mode is detected.

   d) Experimentally find the R_{TON} resistor value (between $R_{TON.min}$ and $R_{TON.max}$) that optimizes efficiency at the light-load level (10% and 25% of load).

   The adaptive gate-driver is effective of course when the circuit operates out of the burst -mode; furthermore, the efficiency improvement is more impacting in applications which operate at higher switching frequency and use bigger SR MOSFETs (i.e. with greater gate charge).

1.5 VAUX pin usage

In charger applications operating in the CC regulation, the output voltage V_{OUT} (which is also used to supply the SRK1000) may considerably decrease while the output current is kept constant at progressively reduced load impedance. For example, a 10 W charger, set at the +5 V output in the CV regulation, may be required to operate down to the 2 V output while it is regulating the output current to somewhat more than 2 A in the CC regulation.

In order to guarantee the SR MOSFET switching even with low VCC supply voltage, the SRK1000 is provided with the VAUX pin. Referring to the schematic in *Figure 9*, when the VCC voltage decreases below the threshold $V_{CC\_SO\_On}$ (> V_{CC_Off}), an internal switch is turned on allowing the capacitor C2 placed on the VCC pin to be charged up to the turn-on threshold V_{CC_On} by a current drawn through the VAUX pin.

The VAUX pin may be connected, for example, to the rectified SR MOSFET drain voltage, like shown in *Figure 9* or to another auxiliary voltage of the flyback transformer, like indicated in the schematic of *Figure 10*.

Figure 9. VAUX supply from rectified SR MOSFET drain

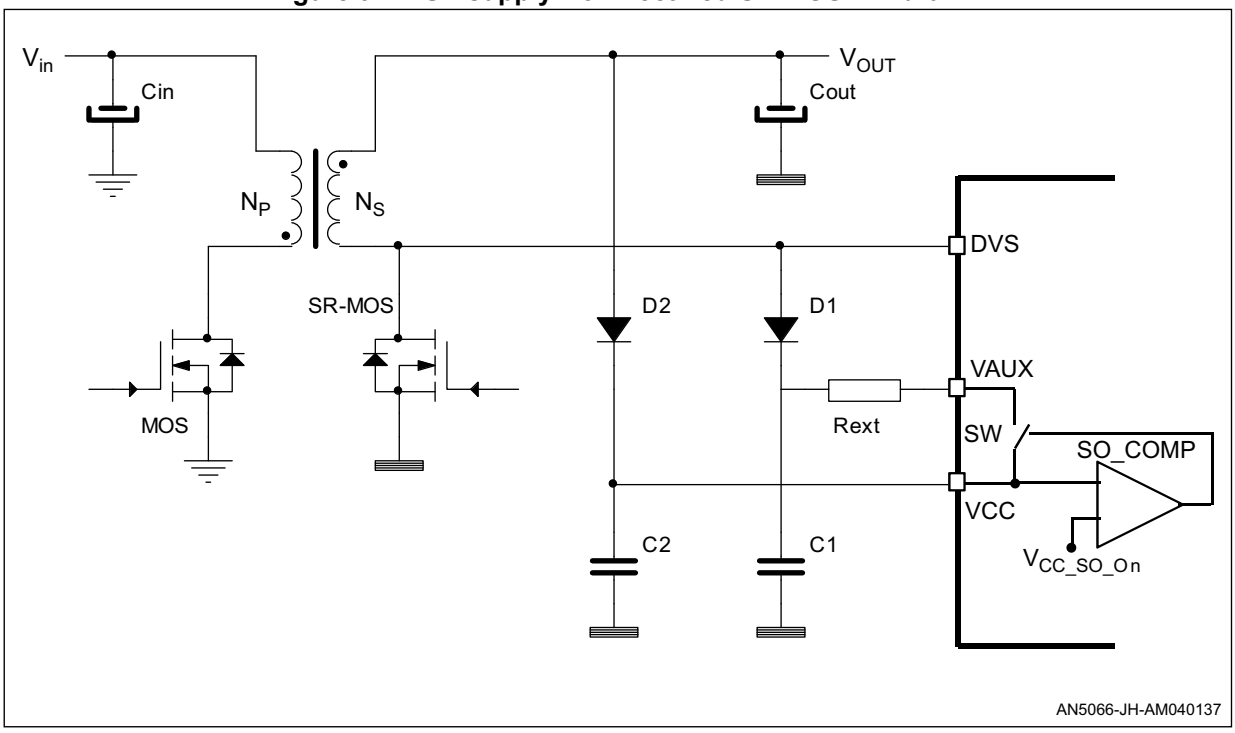
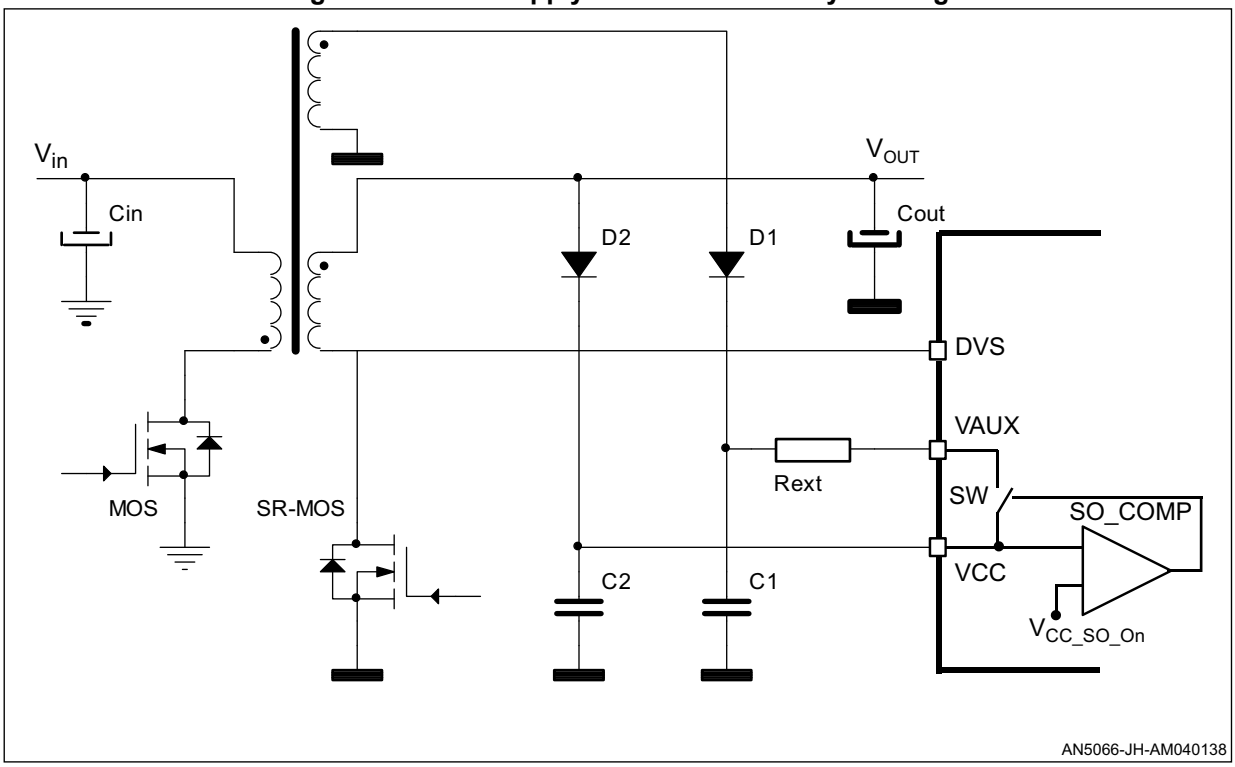


Figure 10. VAUX supply from other auxiliary winding



In either cases, a (Schottky) decoupling diode (D2) is necessary to avoid the VAUX pin may charge the output capacitor. An external resistor R_{ext} may be used in series to the VAUX pin in order to dissipate externally some power amount that, without that resistor, would be totally dissipated inside the SRK1000.

Considering the circuit in *Figure 9*, the following exemplification is provided to calculate the value of the R_{ext} resistor and power dissipation, in the case of a +5 V charger with operation down to 2 V in the CC regulation and transformer secondary-to-primary reflected voltage of 75 V:

1. Measure or estimate the IC current consumption during the CC regulation operation as below:

Equation 1

$$I_{CC} = I_{q\_run} + V_{CC\_avg} \cdot C_{iss} \cdot F_{sw} = 0.7\ mA + 4.1\ V \cdot 5\ nF \cdot 50\ kHz = 1.725\ mA$$

where I_{q_run} is the IC quiescent current, V_{cc_avg} is the average voltage across the VCC pin (mean value between V_{CC_On} and $V_{CC\_SO\_On}$), C_{iss} is the SR MOSFET input capacitance and F_{sw} is the switching operating frequency during the CC regulation.

2. Calculate the maximum and minimum voltage available at the VAUX pin:

Equation 2

$$V_{AUX\_min} = V_{o.CC} + V_{in.min} (N_S/N_P) - V_F = 2\ V + 75\ V\ (1/15) - 0.35\ V = 6.65\ V$$

$$V_{AUX\_max} = V_{o.CC} + V_{in.max} (N_S/N_P) - V_F = 2\ V + 375\ V\ (1/15) - 0.35\ V = 26.65\ V$$

where $V_{o.CC}$ is the output voltage in the CC regulation, $V_{in.min}$ / $V_{in.max}$ is the converter minimum/maximum input dc voltage, N_S/N_P is the transformer turn ratio, and V_F is the voltage drop of D1.

3. Calculate the power dissipation of the SRK1000, including device consumption and driving:

Equation 3

$$P_{d\_CC} = V_{cc\_avg} \cdot I_{CC} = 4.1\ V \cdot 1.725\ mA = 7.072\ mW$$

where V_{CC_On} is the IC turn-on threshold and $V_{CC\_SO\_On}$ is the VAUX switch activation threshold.

4. Calculate the maximum external resistance in series to the VAUX pin:

Equation 4

$$R_{ext\_MAX} = (V_{AUX\_min} - V_{CC\_On}) / I_{CC} - R_{on} = (6.65\ V - 4.3\ V) / 1.725\ mA - 40\ \Omega = 1.322\ k\Omega$$

$$\text{choosing } R_{ext} = 1.2\ k\Omega \Rightarrow R_{tot} = R_{ext} + R_{on} = 1.2\ k\Omega + 40\ \Omega = 1.24\ k\Omega$$

where *Ron* is the resistance of the internal VAUX switch.

5. Calculate the maximum and minimum current from the VAUX pin:

Equation 5

$$I_{AUX\_min} = (V_{AUX\_min} - V_{CC\_On}) / R_{tot} = (6.65\ V - 4.3\ V) / 1.24\ k\Omega = 1.89\ mA$$

$$I_{AUX\_max} = (V_{AUX\_max} - V_{CC\_On}) / R_{tot} = (26.65\ V - 4.3\ V) / 1.24\ k\Omega = 18.02\ mA$$

6. Calculate the maximum power dissipation from VAUX at maximum input voltage ($V_{in.max}$):

Equation 6

$$P_{d\_AUX} = V_{AUX\_max} \cdot I_{CC} = 26.65\ V \cdot 1.725\ mA = 45.971\ mW$$

7. Calculate the maximum power dissipation on external resistance and inside the SRK1000:

Equation 7

$$P_{d\_Rext} = (P_{d\_AUX} - P_{d\_CC})\ R_{ext} / R_{tot} = (45.971\ mW - 7.072\ mW)\ 1.2\ k\Omega / 1.24\ k\Omega = 37.64\ mW$$

$$P_{d\_SRK} = P_{d\_AUX} - P_{d\_Rext} = 45.971\ mW - 37.64\ mW = 8.33\ mW$$

2 Electrical schematic description

The board electrical schematic is shown in *Figure 11*: it refers to the generic evaluation board in *Table 1 on page 1* (all the boards have similar schematics, only differing in the SR MOSFET part number).

The selected SR MOSFETs in the various boards are 100 V rated devices and basically they are supposed to operate in applications with the output voltage up to 12 V, used also to supply the SRK1000 on the VCC pin. For applications at the 5 V output voltage, the logic level SR MOSFET is provided in the PowerFLAT package.

Technical positions for an RC snubber across the SR MOSFET are provided on the PCB layout (R3 - C3 not mounted) so that the user can set the values more suitable to dump the ringing across the MOSFET drain-source and reduce its peak voltage in the particular application.

The boards are provided to operate in QR flyback applications (no capacitor on TON pin). In case of mixed DCM-CCM applications, a 100 pF capacitor mounted in the technical position C4 can be used to fit this operating mode.

The programmed blanking after the turn-on is 800 ns (R5 = 68 kΩ). According to specific application needs, it can be set to any other value in 0.4 - 3 µs range, by using the proper resistor value across the TON pin, using the following relationship:

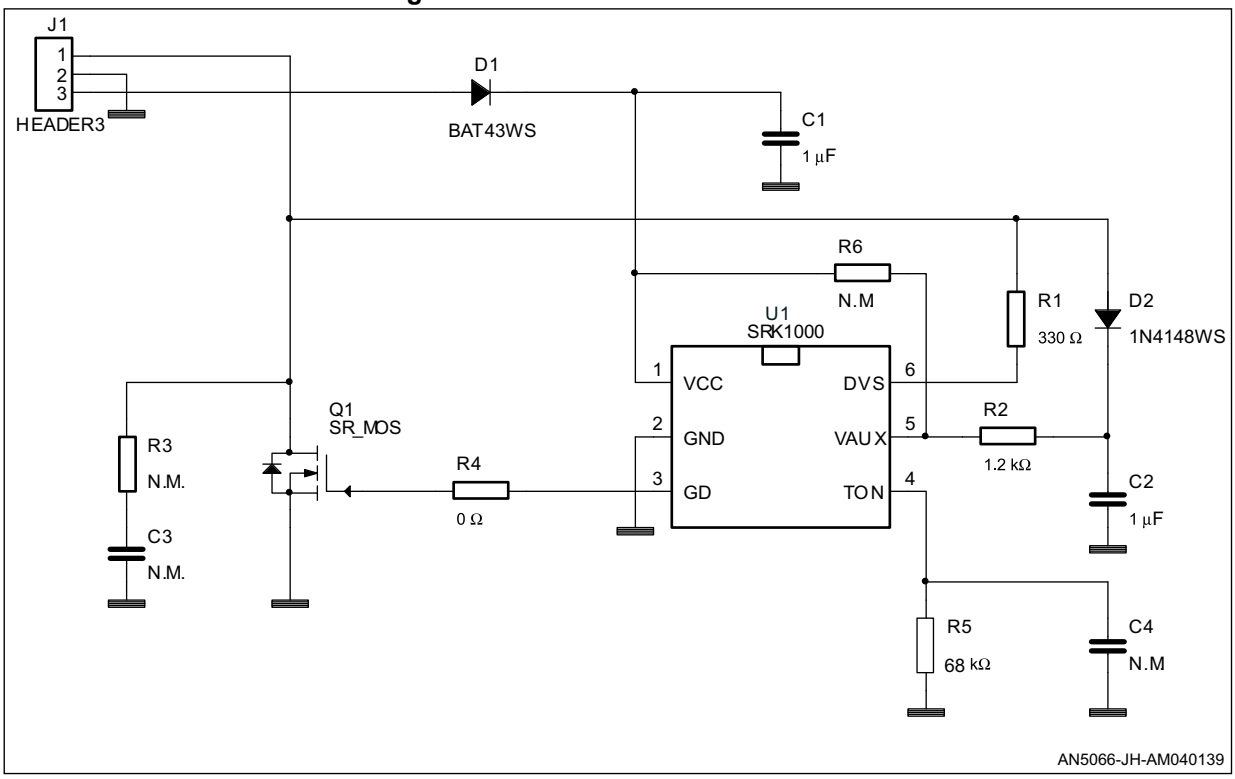
Equation 8

$$T_{ON\_MIN} = 12 \cdot 10^{-12} R_{TON} \qquad \text{with } R_{TON} \text{ ranging in [33 k}\Omega \text{ - 250 k}\Omega\text{]}$$

The resistor R1 (= 330 Ω) in series to the DVS pin is required in order to limit dynamic current injections in any condition.

No resistor is required in series between the GD pin and the SR MOSFET gate terminal. The signal on the GD pin is internally used to detect on the falling edge the time instant where the body diode starts conducting (after the turn-off) and a series resistor would affect the target residual conduction duration of the body diode T_{diode_off}. In any case, a direct connection of the GD pin to the MOSFET gate terminal maximizes efficiency and does not affect EMI. In fact the SR MOSFET is turned on only after the current starts flowing through the body diode, when the drain voltage has already dropped to $-V_F$; therefore the turn-on just causes a voltage step from $-V_F$ to the drop across the channel resistance ($-R_{ds\_ON} \cdot I_{SR}$) with a negligible impact on EMI. The same considerations are true also after the turn-off, where the current passes again through the body diode.

Figure 11. Board electrical schematic



The boards are provided with the VAUX pin connected to a RCD circuit (that rectifies the SR MOSFET drain-source voltage), suitable in the charger application (in order to allow the operation of the SRK1000 controller also when the output voltage reduces during the CC regulation operation).

In case of an adapter circuit (without the CC regulation operation), the RCD circuit (R2, C2, D2) can be removed, the diode D1 can be substituted by a jumper while a zero ohm resistor needs to be added in the position R6 (on the PCB back side), to connect the VAUX and VCC pins (required when VAUX functionality is not used).

The bill of material of the EVL-SRK1000 boards (in *Table 2*) are all identical, differing only for the MOSFET part number and controller option.

Since the PCB for the SRK1000A and SRK1000B is exactly the same used for the SRK1000 (the same silkscreen), in order to easily recognize the controller part number mounted on the board, a blue sticker or a yellow sticker is provided on the board back side for SRK1000A and SRK1000B, respectively.

Table 2. EVL-SRK1000 bill of material

Ref.	Value / PN	Description	Supplier	Case
C1	1 µF	50 V CERCAP X7R - general purpose	BC Components	SMD 0805
C2	1 µF	100 V CERCAP X7R - FIEXITERM series	AVX	SMD 1206
C3	N.M.	100 V CERCAP X7R - general purpose	BC Components	SMD 1206
C4	N.M.	50 V CERCAP X7R - general purpose	BC Components	SMD 0805
D1	BAT43WS	Small signal Schottky diode	VISHAY	SOD323
D2	1N4148WS	Small signal fast switching diode	VISHAY	SOD323
Q1	SR MOSFET	N-channel power MOSFET	-	-
R1	330 Ω	SMD std. film res. - 1/8 W - 1% - 200 ppm/°C	BC Components	SMD 0805
R2	1.2 kΩ	SMD std. film res. - 1/4 W - 5% - 250 ppm/°C	BC Components	SMD 1206
R3	N.M.	SMD std. film res. - 1/4 W - 5% - 250 ppm/°C	BC Components	SMD 1206
R4	0 Ω	SMD std. film res. - 1/8 W - 5% - 250 ppm/°C	BC Components	SMD 0805
R5	68 kΩ	SMD std. film res. - 1/8 W - 1% - 200 ppm/°C	BC Components	SMD 0805
R6	N.M.	SMD std. film res. - 1/8 W - 5% - 250 ppm/°C	BC Components	SMD 0603
U1	SRK1000 (A-B)	Adaptive SR. flyback controller	STMicroelectronics	SOT23-6

How to implement the board in the converter

The evaluation board is intended to implement synchronous rectification in an existing flyback converter in the low-side configuration (i.e. replacing the output rectifier with the SR MOSFET in the configuration with the anode of its body diode connected to the secondary ground), like indicated in *Figure 12*. In this case, referring to the connector J1 in the board schematic: the pin 1 has to be connected to the transformer terminal, the pin 2 has to be connected to secondary ground, while the pin 3 has to be connected to the output voltage.

The evaluation board can be used also in the high-side configuration (see *Section 1.3 on page 9*). In this case, the implementation is done by replacing the output rectifier with the SR MOSFET in the configuration with the cathode of its body diode connected to the output voltage, like indicated in *Figure 13*: the pin 1 of the connector J1 has to be connected to the output voltage, the pin 2 to the transformer. The VCC supply to the SRK1000 has to be provided externally, between the pin 3 and pin 2 of the connector J1, for example, through a further transformer winding. The VCC supply can be provided also by adding some components on the evaluation board like in *Figure 14*.

In this case, the implementation is like in *Figure 13*: the pin 1 and pin 2 of the connector J1 are soldered to the board, while the pin 3 remains unconnected. The further components for the VCC supply have to be added by rework (there is no technical position foreseen on the PCB).

Figure 12. Implementing the board on existing flyback converter (low-side configuration)

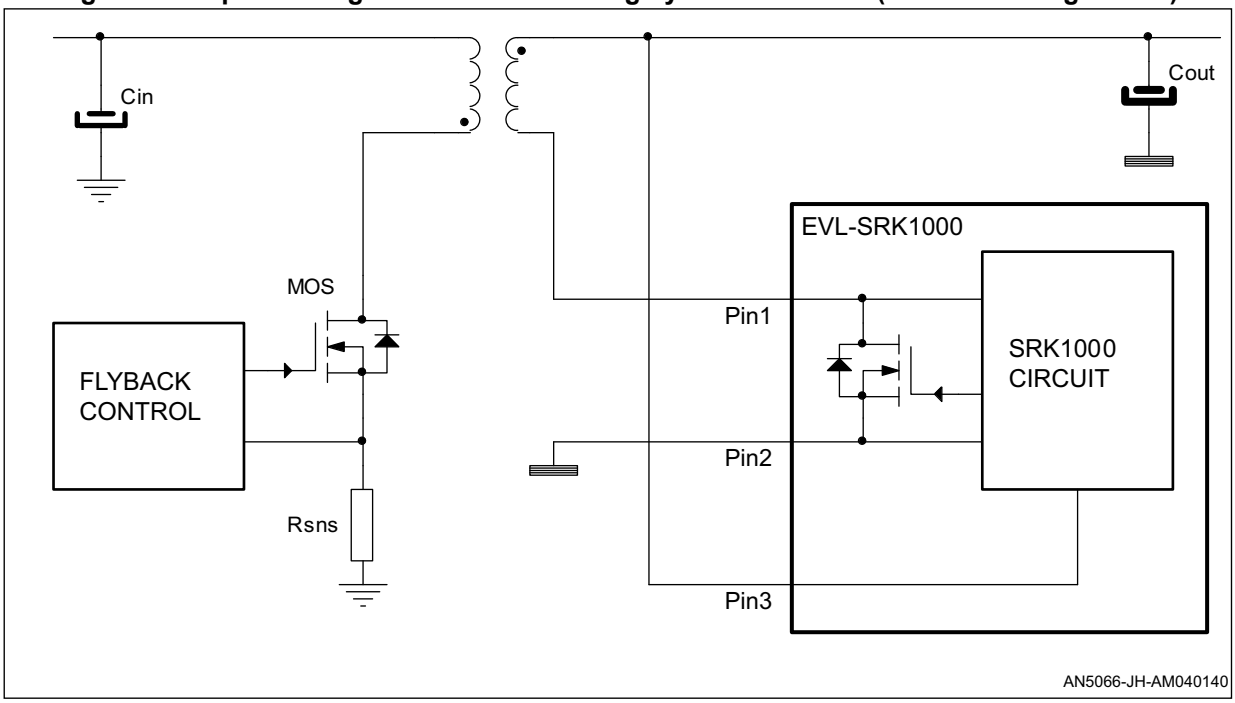


Figure 13. Implementing the board in high-side configuration

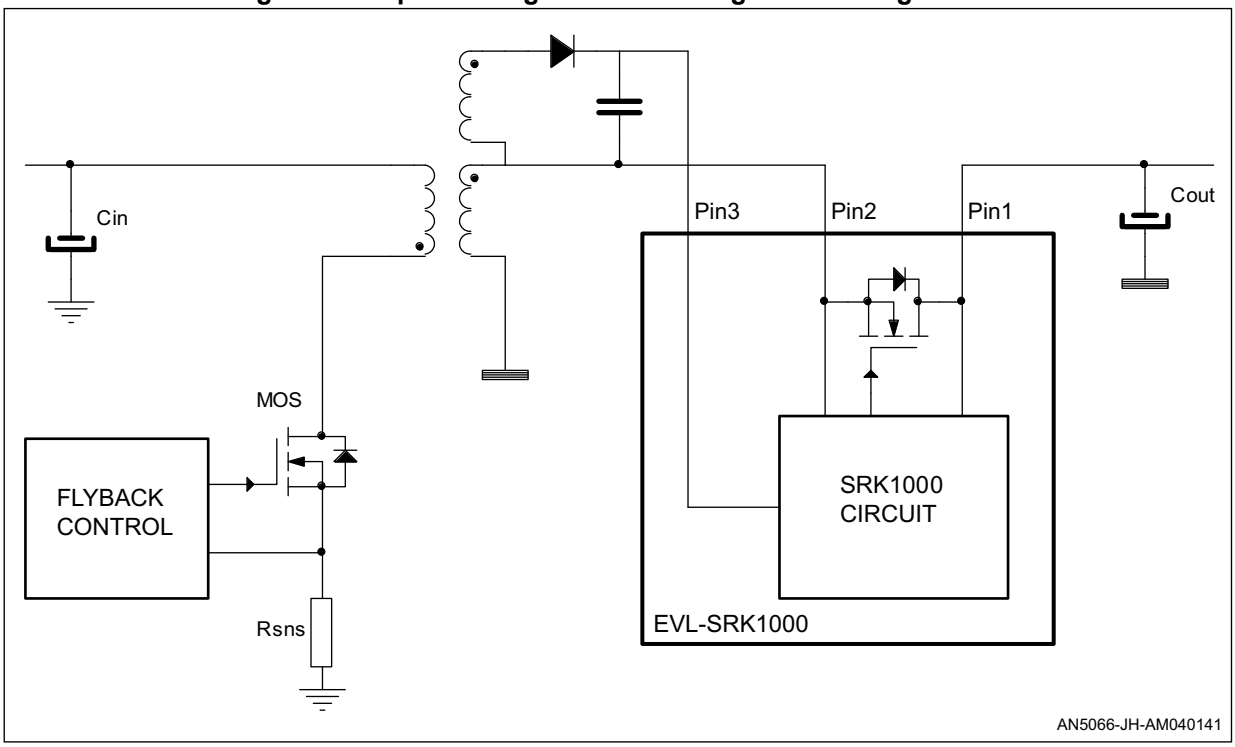
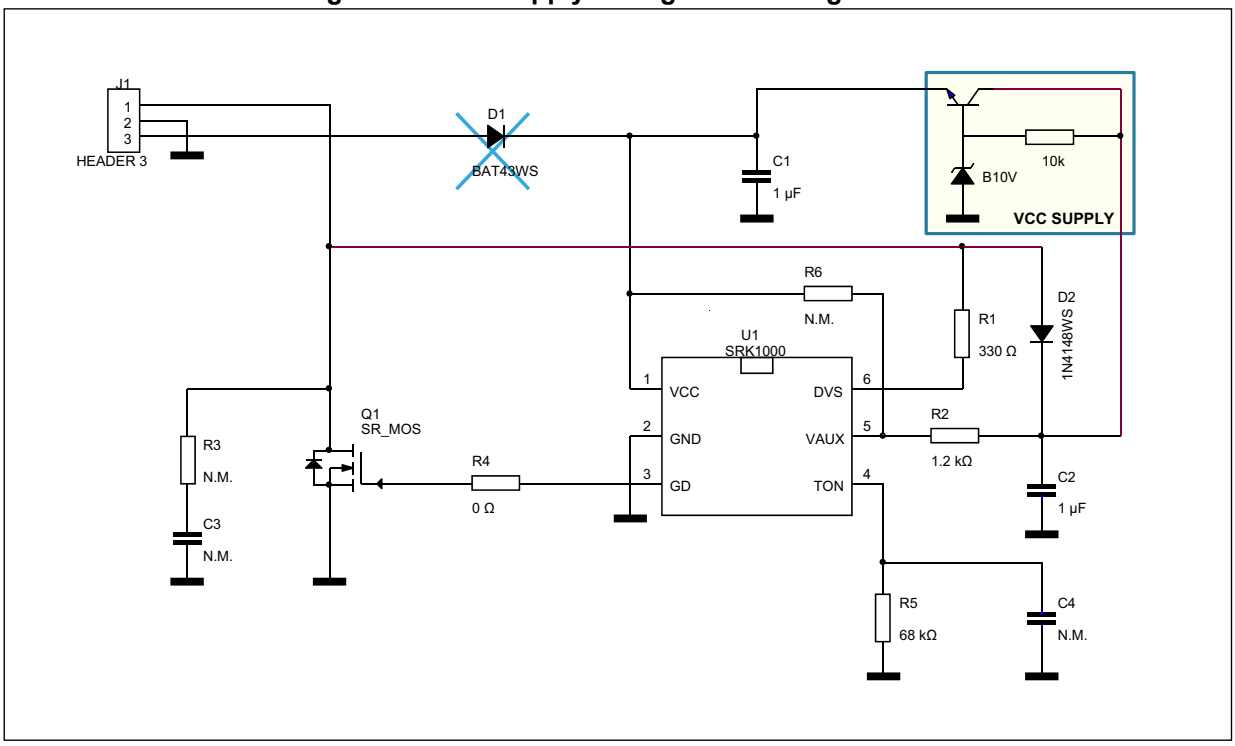


Figure 14. VCC supply for high-side configuration



3 Power losses and thermal design

The SR dramatically reduces the output rectification power losses enabling the design of more efficient power supplies and, even more significant, with a considerable reduction of the converter secondary side size.

To get a better idea of the improvement obtained by implementing the SR with the SRK1000, the power loss calculation in a 12 V, 36 W output power, quasi-resonant flyback application is illustrated below, comparing diode and MOSFET losses.

3.1 Power losses calculation

The data used for calculations are:

Output voltage and power: V_o = 12 V P_o = 36 W

Transformer primary inductance: L_p = 700 µH

Transformer turn ratio: n = 9.4

Period of ringing after demagnetization: T_{Res} = 2.5 µs

Efficiency and forward drop: η = 0.9 V_F = 0.3 V

The formulas used to calculate the secondary peak and rms currents are shown in *Figure 15* and provide the following results at dc input voltage levels of 150 V and 300 V:

At 150 Vdc: I_{pk_s} = 12.52 A I_{rms_s} = 5.21 A

At 300 Vdc: I_{pk_s} = 10.24 A I_{rms_s} = 4.71 A

Figure 15. Formulas for calculations

- Transition frequency:
$$f_T = \frac{1}{2\,\frac{P_o}{\eta} L_p \left[\frac{1}{V_{dc}} + \frac{1}{n(V_o + V_f)}\right]^2}$$

- Switching frequency and period:
$$f_{sw} = \frac{4\,f_T}{(1+\sqrt{1+2f_T T_{Res}})^2} \qquad T_{sw} = \frac{1}{f_{sw}}$$

- Primary and secondary peak current and demagnetization time:
$$I_{pk} = \sqrt{\frac{2P_o}{\eta L_p f_{sw}}} \qquad I_{pk\_s} = nI_{pk} \qquad T_{Dem} = \frac{L_p I_{pk}}{n(V_o + V_f)}$$

- Secondary rms current value:
$$I_{rm\_s} = I_{pk\_s}\sqrt{\frac{T_{Dem}}{3T_{sw}}}$$

To evaluate power losses, the suitable diode rectifier and MOSFET part numbers have been selected. In case of diode rectification, the FERD20U60DJFD has been chosen. The power losses associated to this rectifier can be calculated using the formula indicated in the diode datasheet (see *2.* in *Section 5: References on page 26*) (which takes into account both of the diode forward drop V_F = 295 mV and of the dynamic resistance effect R_d = 10.5 mΩ):

Equation 9

$$P_{Diode} = V_F \cdot I_o + R_D \cdot I_{rms\_s}^2$$

In case of SR, the selected MOSFET is the STF80N10F7 (see *3.* in *Section 5: References*) (TO220F package with channel resistance R_{DS_on} = 10 mΩ max. and the temperature coefficient at 100 °C k_T = 1.5). Switching losses associated to the MOSFET turn-on are negligible because each MOSFET is turned on after its body diode starts conducting. Also switching losses at the turn-off are of minor concern because, after the MOSFET is turned off, the current still goes on flowing through the body diode.

Thanks to adaptive turn-on and turn-off algorithms, the SR MOSFET conduction angle is maximized so that losses associated to the current flowing through the body diodes (before the turn-on and after turn-off) can be neglected too. Therefore, the most part of SR MOSFET losses can be summarized into conduction losses; therefore the SR MOSFET power dissipation is ideally calculated by:

Equation 10

$$P_{MOS} = k_T \cdot R_{DS\_on} \cdot I_{rms\_s}^2$$

3.2 IC consumption and driving losses calculation

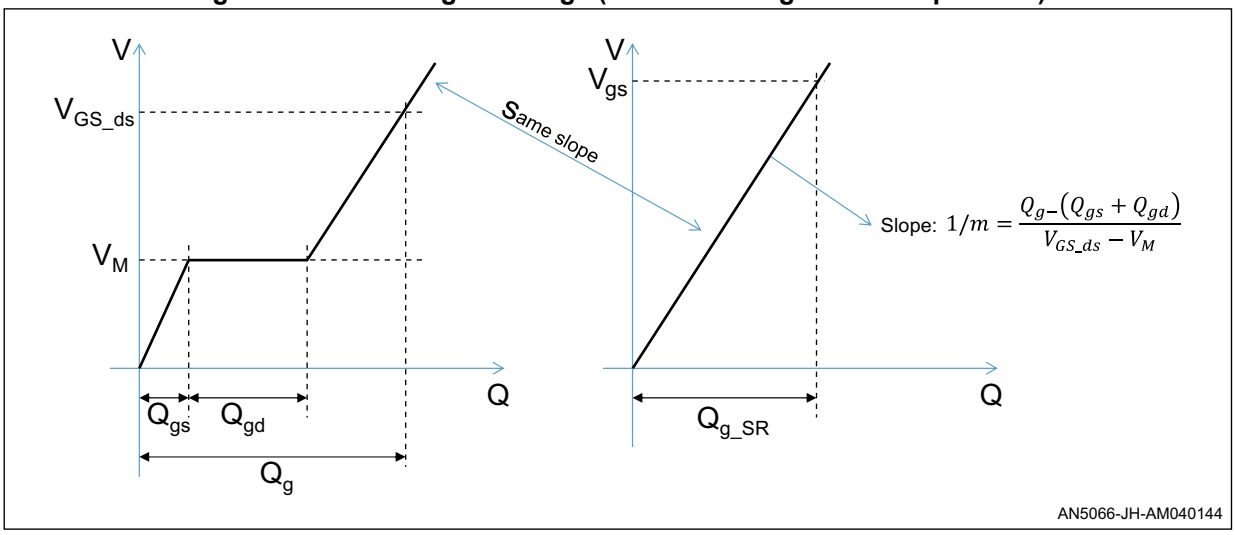
The power consumption of the SRK1000 and the driving losses must be taken into account: for a rough estimation, we can consider the IC quiescent current indicated in the datasheet (I_q) and the energy per cycle required for SR MOSFET driving (E_{ZVS}).

Figure 16 shows the curve of the MOSFET gate charge versus the gate-source voltage:

- The part on the left is related to the MOSFET operated in hard switching
- The part on the right is related to the MOSFET operated in ZVS, like in the case of the SR application

Note that, in the SR application, the MOSFET has no Miller effect both at the turn-on and at turn-off.

Figure 16. MOSFET gate charge (hard switching and ZVS operation)



From *Figure 16*, the gate charge for each SR MOSFET of the application can be found as follows, at a generic gate-source voltage V_{gs}:

Equation 11

$$Q_{g\_SR}(V_{gs}) = V_{gs}\frac{Q_g - (Q_{gs} + Q_{gd})}{V_{GS\_ds} - V_M}$$

Where V_{gs} is the gate-source generic level, V_M is the Miller plateau voltage (i.e. the voltage of the flat part in the left plot of *Figure 16*) and Q_g, Q_{gd}, Q_{gs} are the charges associated to MOSFET gate driving, specified in the MOSFET datasheet at a fixed gate-source voltage V_{GS_ds}.

In some cases, the MOSFET datasheet directly provides for the gate charge data related to SR applications, generally indicated as Q_{sync}, at a fixed V_{GS_ds} voltage (usually 10 V or 4.5 V); in this case, the gate charge at a generic V_{gs} can be found as:

Equation 12

$$Q_{g\_SR}(V_{gs}) = V_{gs}\frac{Q_{sync}}{V_{GS\_ds}}$$

In cases where only the MOSFET input capacitance is known, the gate charge at a generic V_{gs} can be found as:

Equation 13

$$Q_{g\_SR}(V_{gs}) = V_{gs} \cdot C_{in}$$

where C_{in} is basically the summation of the MOSFET gate-source capacitance C_{gs} and of the gate-drain capacitance C_{gd}.

The above expression of the gate charge allows finding the energy per cycle required for SR MOSFET driving:

Equation 14

$$E_{ZVS}(V_{gs}) = V_{CC} \cdot Q_{g\_SR}(V_{gs})$$

where V_{CC} (= V_o) is the IC supply voltage. From *Equation 11* and *Equation 13*, the calculation of the total gate charge and the energy per cycle required for MOSFET driving is done, referring to the IC and application data in *Table 3* and using STF80N10F7 gate charge data in *Figure 17*:

$$Q_{g\_SR} = 37 \text{ nC} \qquad E_{ZVS} = 0.45 \text{ µJ}$$

and finally the above calculated energy per switching cycle allows to calculate the total IC consumption and driving power, according to the following expression:

Equation 15

$$P_{SRK} = V_{dd} \cdot I_q + E_{ZVS}(V_{gs}) \cdot f_{sw}$$

At 150 Vdc: $P_{SRK} = 36$ mW

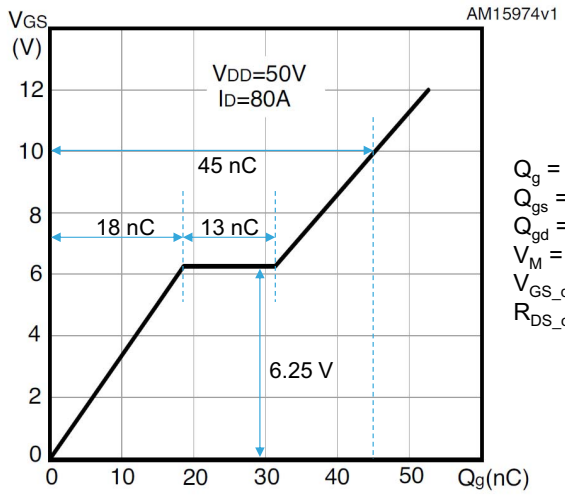
At 300 Vdc: $P_{SRK} = 50$ mW

The power calculated for the two above cases (neglecting MOSFET internal gate resistance) is almost completely dissipated inside the SRK1000.

Table 3. IC and application data

Data	Description
$V_{CC} = V_o = 12$ V	IC supply voltage (= Vout)
$V_{gs} = V_{gd\_high} = 10$ V	Gate-driver high level voltage
$I_q = 600$ µA	Current consumption in run mode (excluding driver current)
$f_{sw} = 64$ kHz	Operating frequency at 150 Vdc
$f_{sw} = 96$ kHz	Operating frequency at 300 Vdc

Figure 17. STF80N10F7 gate charge data



Q_g = 45 nC — typical total gate charge @ V_{GS_ds}
Q_{gs} = 18 nC — typical gate-source charge @ V_{GS_ds}
Q_{gd} = 13 nC — typical gate-drain charge @ V_{GS_ds}
V_M = 6.25 V — Miller plateau voltage (from plot)
V_{GS_ds} = 10 V — V_{GS} for charge values on datasheet
R_{DS_on} = 10 mΩ — max ON resistance @ 25°C

STF80N10F7

Finally, at the full load the total power saving obtained by implementing SR with respect to the diode rectification is calculated as follows:

Equation 16

$$\Delta P = P_{Diode} - (P_{MOS} + P_{SRK})$$

At 150 Vdc: $\Delta P = 0.727$ W

At 300 Vdc: $\Delta P = 0.735$ W

A power saving of 0.73 W corresponds to a 2% efficiency boost in this 36 W application.

3.3 Thermal design consideration

Considering for the SRK1000 a maximum thermal rise of 65 °C, in the worst case of *Equation 15*, the maximum junction to ambient thermal resistance allowed is:

Equation 17

$$R_{th(j-amb)} = \frac{65°C}{P_{SRK}} = 1300°C/W$$

This value is much higher than the junction to ambient thermal resistance of the SRK1000 in the datasheet ($R_{th\ j\text{-}amb}$ = 200 °C/W) and this means that the device can easily manage that power dissipation.

A straightforward calculation of the junction temperature increases from the the calculated power dissipation and from junction to ambient thermal resistance $R_{th\ j\text{-}amb}$ (JEDEC definition) in the datasheet leads to:

Equation 18

$$\Delta T_j = R_{th\ j\text{-}amb} \cdot P_{SRK} = 10\ °C$$

Anyway, the junction temperature obtained from the above calculated temperature increase above ambient temperature is not a reliable data, since the heat generated internally to the IC is dissipated not only through the device package, but also through the copper track connected to the GND pin, while in the JEDEC definition of $R_{th\ j\text{-}amb}$ heat is only dissipated through the package. Therefore, the real junction temperature should be somewhat lower than the calculated one.

Considering instead the junction/case top thermal resistance, $R_{th\ j\text{-}case}$ = 60 °C/W (where the generated heat is dissipated both through the package and through the pins and therefore strongly depends on the PCB copper area), more realistic junction temperature can be estimated. By measuring the temperature on the top of the SRK1000 package, the device junction temperature can be calculated as follows (supposing the temperature measured on the case top is T_{case} = 100 °C):

Equation 19

$$T_j = T_{case} + R_{th\ j\text{-}case} \cdot P_{SRK} = 103\ °C$$

It is worth noticing that the IC junction/case top thermal resistance in the datasheet refers to a copper area connected to the SRK1000 GND pin of 10 mm^2 and the thickness of 35 µm, with the FR4 PCB material, 1.6 mm thickness.

4 Layout suggestions

The GND pin is the return of the bias current of the device and the return for the gate-drive current: it should be routed in the shortest way as possible to the common point where the source terminal of the SR MOSFET and output capacitor negative terminal are connected. When laying out the PCB, care must be taken in keeping the source terminal of the SR MOSFET as close to the output capacitor negative terminal as possible.

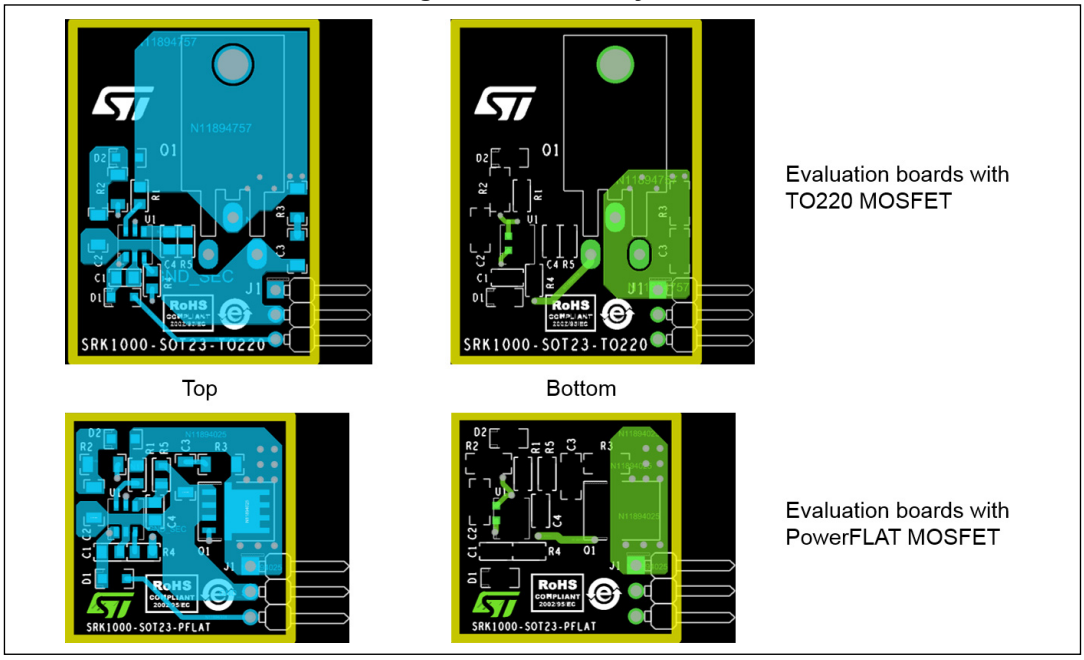
The usage of bypass capacitors between the VCC pin and GND pin is recommended. They should be low-ESR, low-ESL type and located as close to the IC pins as possible. Sometimes, a series resistor (in the tens Ω) between the converter's output voltage and the VCC pin, forming an RC filter along with the bypass capacitor, is useful to get a cleaner VCC voltage.

A larger copper area connected to the GND pin and located below the device package helps heat dissipation generated inside the IC, keeping lower junction temperature.

Below the main recommendations that should be taken into account designing the PCB:

- Connect the device GND pin as close as possible to the SR MOSFET source terminal.
- Reduce as much as possible the driving current path length/area.
- Use a bypass capacitor across VCC and GND as close to device pins as possible.
- Use a resistor (> 300 Ω) in series to the DVS pin.
- The DVS connection to the SR MOSFET drain terminal is not critical (since the adaptive turn-off algorithm automatically compensates for stray inductances in the SR MOSFET current path); nevertheless, it should be preferred to sense the MOSFET voltage as close to its drain terminal as possible.
- Since the TON pin sourced current is relatively low, this pin may be affected by current injections coming from close tracks with high dV/dt (i.e. drain sense signals); therefore, the TON pin should be kept away from SR MOSFET drain tracks, with a proper layout.

Figure 18. Board layout



5 References

1. SRK1000 datasheet: available at www.st.com.
2. FERD20U60DJFD datasheet: available at www.st.com.
3. STF80N10F7 datasheet: available at www.st.com.

6 Revision history

Table 4. Document revision history

Date	Revision	Changes
22-Nov-2018	1	Initial release.