Getting started with the EVALSTDRIVE101

Introduction

The EVALSTDRIVE101 is an evaluation board based on the STDRIVE101, a three-phase gate driver, and the STL110N10F7 power MOSFETs.

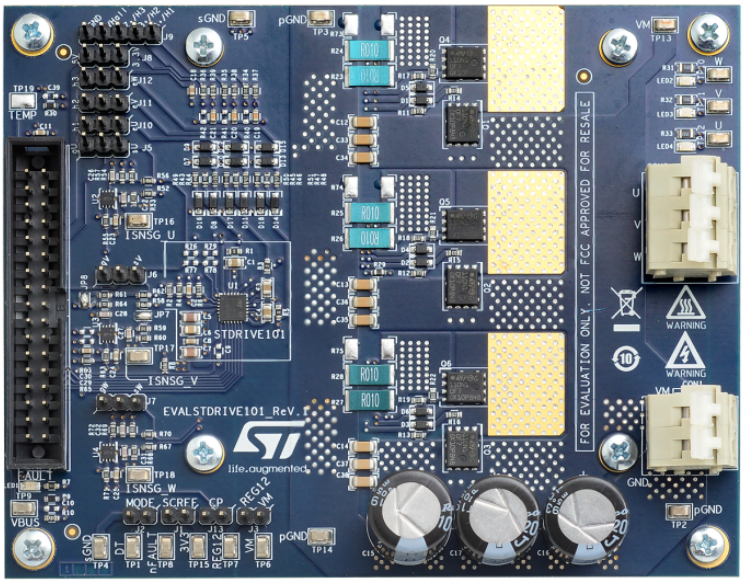
The EVALSTDRIVE101 is designed to drive three-phase brushless motors BLDC and PMSM (Brush Less DC and Permanent Magnet Synchronous Machines); it can be interfaced with different STM32 microcontrollers through the motor control connector.

The board can be configured in single shunt or three-shunt and can support FOC and six-step algorithms in both configurations.

The Hall sensors connector and the phase sensing network present onboard allow to implement both sensor and sensorless algorithms for motion control.

The EVALSTDRIVE101 allows a full evaluation of the STDRIVE101 and its features, including the embedded comparator for overcurrent protection and the drain-source voltage sensing of each power MOSFET.

Figure 1. EVALSTDRIVE101 evaluation board



1 Acronyms and definitons

The description of the items listed in Table 1, can help to understand the acronyms and the definitions used in this document.

Table 1. List of acronyms and definitions

	Description
ADC	Analog to Digital Converter.
BEMF	Back Electromotive Force. It is the voltage generated by each phase of the motor when it is rotating.
BLDC	Brushless DC motor.
FOC	Field Oriented Control: it is a driving algorithm for three-phase motors which allows to control the position of the rotor magnetic field with respect to the stator magnetic field.
Half-bridge	Structure composed by one HS and one LS MOSFET connected together. Refer to Figure 3. Each phase of a three-phase motor is usually driven by a half-bridge structure.
HS	High-side MOSFET. When closed, it connects the load to the positive supply voltage. Refer to Q1, Q2 and Q3 in the schematic represented in Figure 3.
LS	Low-side MOSFET. When closed, it connects the load to the GND. Refer to Q4, Q5 and Q6 in the schematic represented in Figure 3.
MCU	Microcontroller Unit.
Opamp	Operational amplifier.
PCB	Printed Circuit Board.
PMSM	Permanent Magnet Synchronous Machines.
PWM	Pulse Width Modulation: it is a driving technique which uses a square wave with a modulated duty cycle in order to change the amount of current flowing through an inductive load.
Shunt resistor	The shunt resistor is placed on the source of the low-side MOSFET, in order to measure the current flowing in the load. It can be also called “sense resistor”.
Six-step	It is a driving algorithm for three-phase motors which forces the current in two of the three phases of the motor, leaving the third one in high impedance state.

2 Hardware and software requirements

The EVALSTDRIVE101 can be set up to operate with the following hardware and software:

- a microcontroller board compatible with the Motor Control connector
- a custom firmware or a firmware example based on the STM32 Motor Control Software Development Kit (MCSDK), developed on the MCU selected
- A three-phase brushless DC motor with compatible voltage and current ratings
- An external DC power supply

Note: ***Refer to the specific microcontroller board for its hardware and software requirements.***

Two main approaches are available for the MCU controller board:

- an STM32 NUCLEO board coupled with the X-NUCLEO-IHM09M1 adapter
- an STM32 development board embedding the MC control connector

For further information about MCU board availability and firmware examples refer to www.st.com website.

2.1 EVALSTDRIVE101 schematic and BOM

The schematic of the board is represented in the figures from Figure 2 to Figure 6; the bill of material (BOM) is listed in Table 2.

Figure 2. EVALSTDRIVE101 schematic – Driver and MC connector

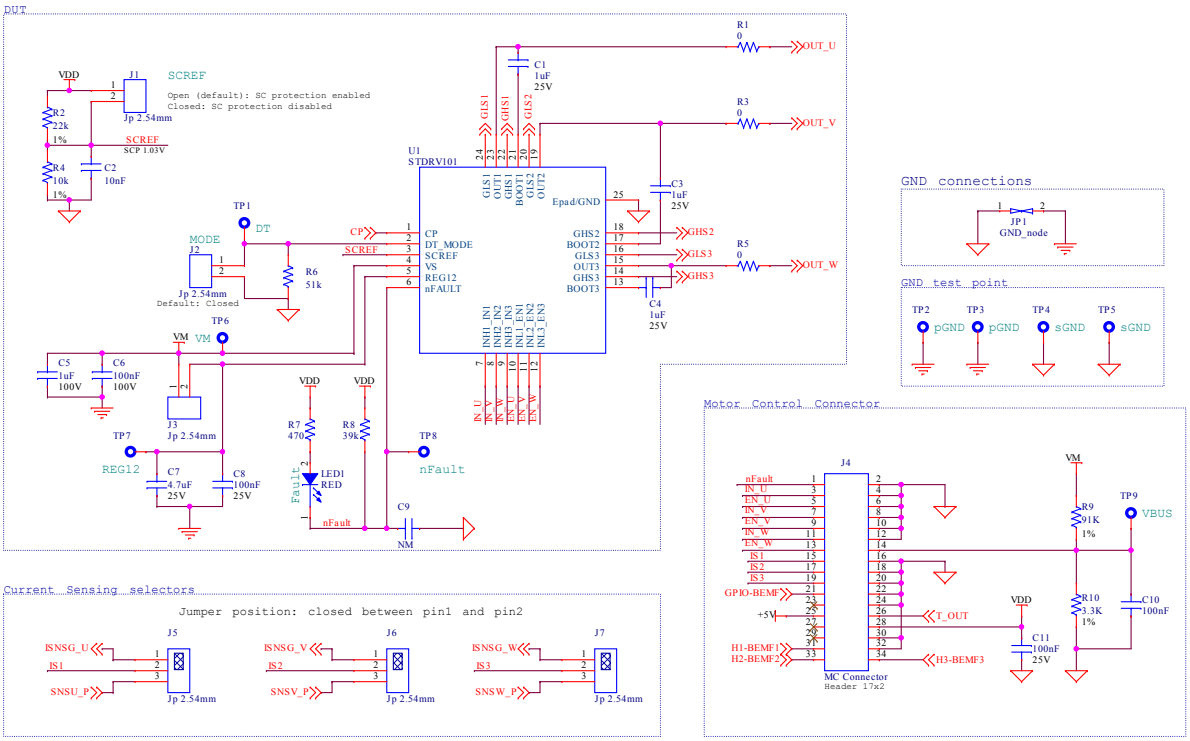


Figure 3. **EVALSTDRIVE101 – Power stage**

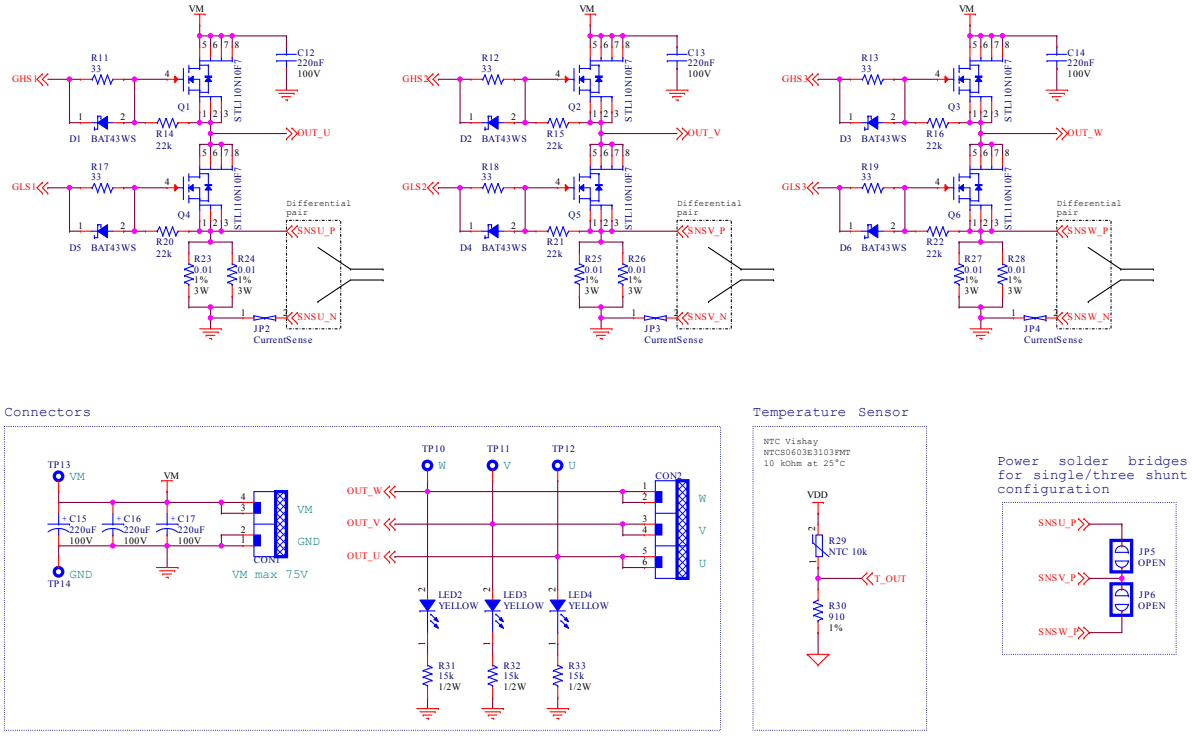


Figure 4. **EVALSTDRIVE101 – Hall sensors/BEMF networks**

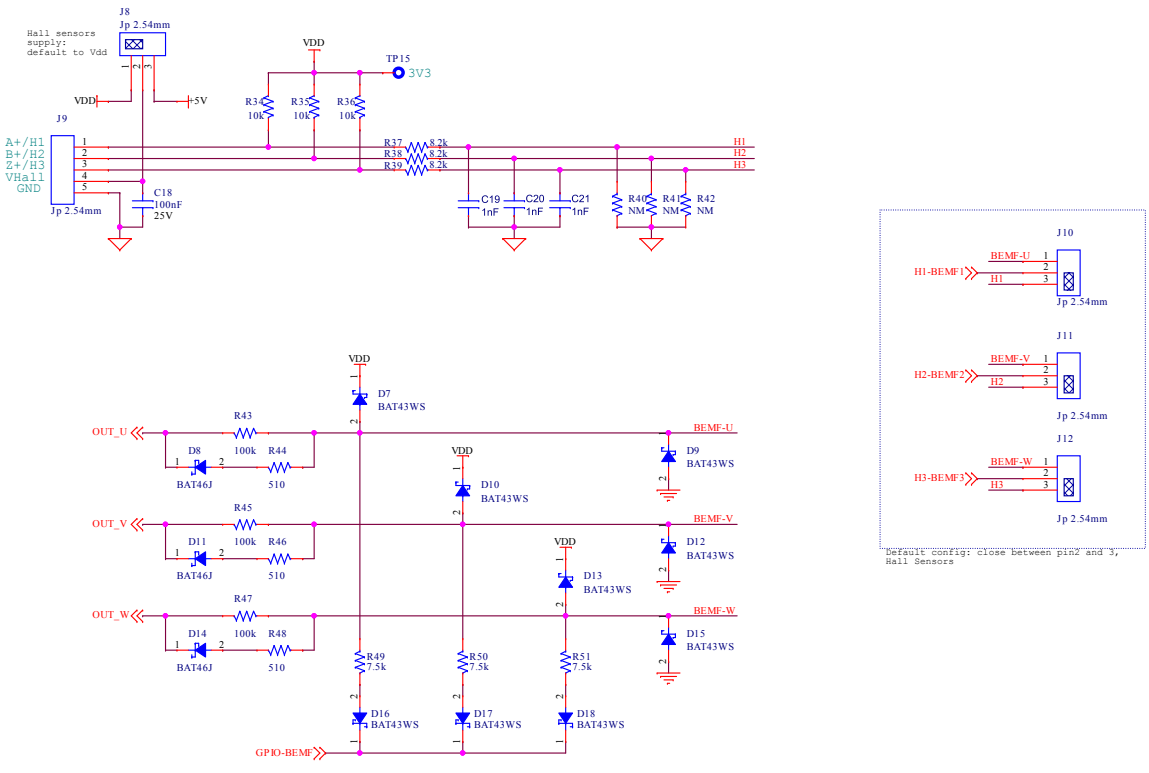


Figure 5. **EVALSTDRIVE101 – Operational amplifiers**

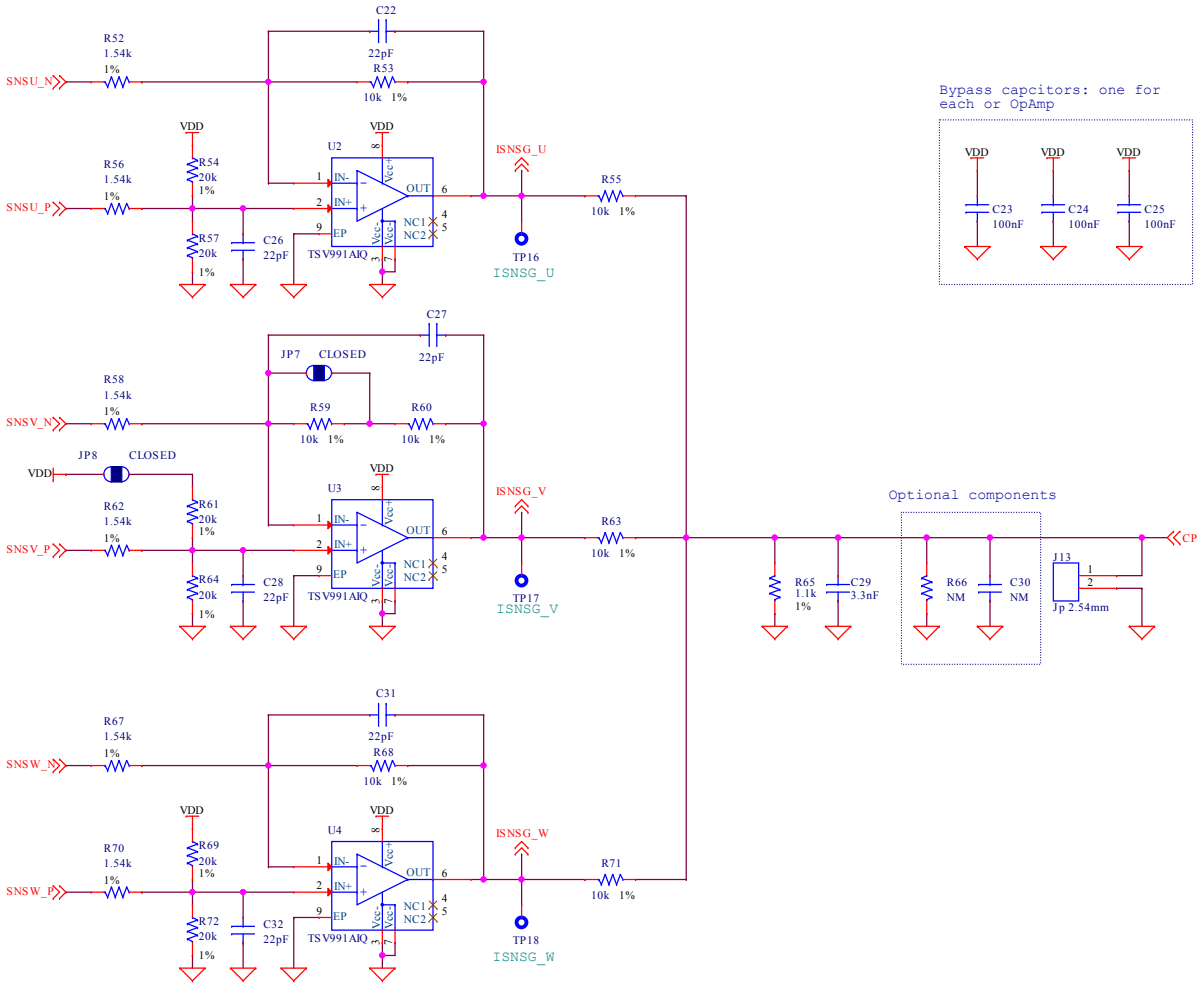
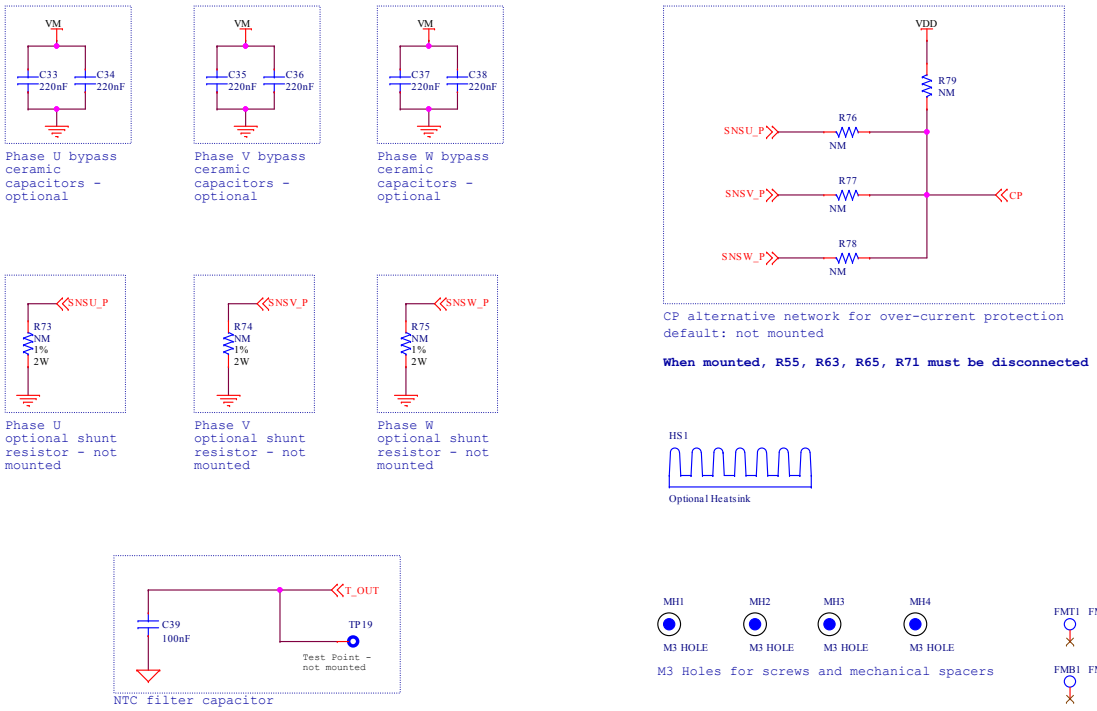


Figure 6. **EVALSTDRIVE101 – Additional components**



2.1.1 Bill of material (BOM)

Table 2. **EVALSTDRIVE101 – Bill of material**

Item	Reference	Value	Part description	Package
1	CON1	2P power connector	20 A power connector	Dual row, 2 poles, pitch 5 mm
2	CON2	3P power connector	20 A power connector	Dual row, 3 poles, pitch 5 mm
3	C1, C3, C4	1 µF, 25 V	SMT ceramic capacitor	Size 0805
4	C2	10 nF, 25 V	SMT ceramic capacitor	Size 0603
5	C5	1 µF, 100 V	SMT ceramic capacitor	Size 0805
6	C6	100 nF, 100 V	SMT ceramic capacitor	Size 0805
7	C7	4.7 µF, 25 V	SMT ceramic capacitor	Size 0805
8	C8, C10, C11, C18, C23, C24, C25, C39	100 nF, 25 V	SMT ceramic capacitor	Size 0603
9	C9, C30	Not mounted	SMT ceramic capacitor	Size 0603
10	C12, C13, C14, C33, C34, C35, C36, C37, C38	220 nF, 100 V	SMT ceramic capacitor	Size 1206
11	C15, C16, C17	220 µF, 100 V	TH electrolytic apacitor	Dia 12.5 mm x 25 mm

Item	Reference	Value	Part description	Package
12	C19, C20, C21	1 nF, 50 V	SMT ceramic capacitor	Size 0603
13	C22, C26, C27, C28, C31, C32	22 pF, 50 V	SMT ceramic capacitor	Size 0603
14	C29	3.3 nF, 50 V	SMT ceramic capacitor	Size 0603
15	D1, D2, D3, D4, D5, D6, D7, D9, D10, D12, D13, D15, D16, D17, D18	BAT43WS	SMT Schottky Diode	SOD-323
16	D8, D11, D14	BAT46J	100V, Small signal Schottky Diode	SOD-323
17	JP1		GND node	
18	JP2, JP3, JP4		Current sense node	
19	JP5, JP6	default: open	Power solder bridge	
20	JP7, JP8	default: closed	Solder bridge	
21	J1, J3, J13	default: open	Jumper	1x2 strip contact pitch 2.54 mm
22	J2	default: closed	Jumper	1x2 strip contact pitch 2.54 mm
23	J4	MC Connector	Header vertical connector 2x17 poles	17x2 connector pitch 2.54 mm
24	J5, J6, J7, J8	default: closed 1-2	Jumper	1x3 strip contact pitch 2.54 mm
25	J10, J11, J12	default: closed2-3	Jumper	1x3 strip contact pitch 2.54 mm
26	J9		Hall sensors connector	1x5 strip contact pitch 2.54 mm
27	LED1	Red	CHIPLED 0805	Size 0805
28	LED2, LED3, LED4	Yellow	CHIPLED 0805	Size 0805
29	Q1, Q2, Q3, Q4, Q5, Q6	STL110N10F7	N-channel 100 V Power MOSFET	PowerFLAT™ 5x6
30	R1, R3, R5	0 Ω	SMT resistor	Size 0603
31	R2	22 kΩ, 1%	SMT resistor	Size 0603
32	R4, R34, R35, R36, R53, R55, R59, R60, R63, R68, R71	10 kΩ, 1%	SMT resistor	Size 0603
33	R6	51 kΩ	SMT resistor	Size 0603
34	R7	470 Ω	SMT resistor	Size 0603
35	R8	39 kΩ	SMT resistor	Size 0603
36	R9	91 kΩ, 1%	SMT resistor	Size 0603
37	R10	3.3 kΩ, 1%	SMT resistor	Size 0603
38	R11, R12, R13, R17, R18, R19	33 Ω	SMT resistor	Size 0603
39	R40, R41, R42, R66, R76, R77, R78, R79	Not mounted	SMT resistor	Size 0603
40	R14, R15, R16, R20, R21, R22	22 kΩ	SMT resistor	Size 0603
41	R23, R24, R25, R26, R27, R28	10 mΩ, 3 W, 1%	SMT resistor	Size 2512

Item	Reference	Value	Part description	Package
42	R29	10 kΩ @ 25°C	SMT NTC resistor	Size 0603
43	R30	910 Ω	SMT resistor	Size 0603
44	R31, R32, R33	15 kΩ, 0.5 W	SMT resistor	Size 0805
45	R37, R38, R39	8.2 kΩ	SMT resistor	Size 0603
46	R43, R45, R47	100 kΩ, 1%	SMT resistor	Size 0603
47	R44, R46, R48	510 Ω	SMT resistor	Size 0603
48	R49, R50, R51	7.5 kΩ, 1%	SMT resistor	Size 0603
49	R52, R56, R58, R62, R67, R70	1.54 kΩ, 1%	SMT resistor	Size 0603
50	R54, R57, R61, R64, R69, R72	20 kΩ, 1%	SMT resistor	Size 0603
51	R65	1.1 kΩ, 1%	SMT resistor	Size 0603
52	R73, R74, R75	Not mounted	SMT resistor	Size 2512
53	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18	TP-SMD	SMT test point	SMD Pad 3.43 x 1.78 mm
54	**U1**	**STDRIVE101**	**Three-phase gate driver**	**QFN 4x4 24L pitch 0,5 mm**
55	U2, U3, U4	TSV991AIQ	Rail-to-rail input/ output operational amplifier	DFN8 2x2
65	HS1		Heatsink, thermal conductive interposer and 4 x M3 screws	75 x 74.6 x 15 mm
66	MH1, MH2, MH3, MH4		4 x M3 screws and spacers	

3 Hardware description and configuration

The main components and connectors of the EVALSTDRIVE101 are shown in Figure 7 and listed in Table 3.

Figure 7. EVALSTDRIVE101 main components and connectors

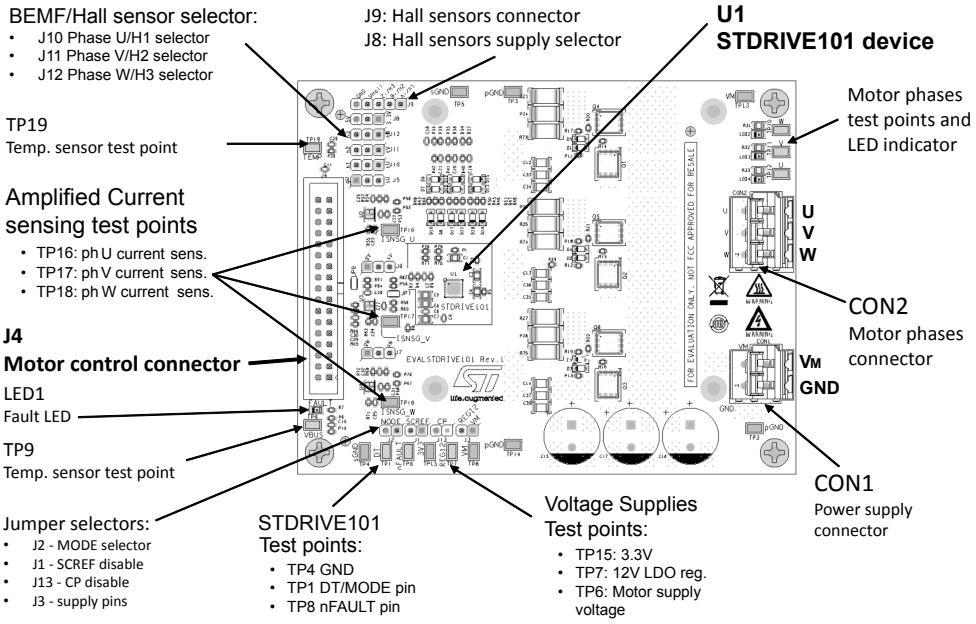


Table 3. EVALSTDRIVE101 configuration jumpers

Ref.	Label	Description	Default
J1	SCREF	Allows to short the SCREF pin of the STDRIVE101 to 3.3V, thus disabling the VDS monitoring protection (see Section 5.2).	Open (SC protection enabled)
J2	MODE	Allows to short the DT/MODE pin of the STDRIVE101 to GND, thus enabling the INH/INL mode. If left open, the STDRIVE101 is configured in EN/IN mode (see Section 5.4).	Closed (INH/INL mode)
J3	REG12	Allows to connect the motor voltage supply (V_M) to the REG12 pin of the STDRIVE101 internal regulator (see Section 5.3).	Open
J4		Motor control connector (see Section 3.1)	
J5		Current sensing selector for phase U. Allows to send to the MCU the amplified/conditioned signal or the raw signal of the shunt resistor (see Section 4.1).	Closed between pin 1 and pin 2
J6		Current sensing selector for phase V. Allows to send to the MCU the amplified/conditioned signal or the raw signal of the shunt resistor (see Section 4.1).	Closed between pin 1 and pin 2
J7		Current sensing selector for phase W. Allows to send to the MCU the amplified/conditioned signal or the raw signal of the shunt resistor (see Section 4.1).	Closed between pin 1 and pin 2
J8		Hall Sensors supply selector (see Section 4.2.1): • Jumper closed between pin1 and pin 2: 3.3 V supply • Jumper closed between pin 2 and pin 3: 5 V supply *Note: both 3.3 V and 5 V supplies come from the control board*	Closed between pin 1 and pin 2
J9		Hall sensors connector and supply (see Section 4.2.1)	
J10		Motor position feedback selector (see Section 4.2): • Jumper closed between pin 1 and pin 2: BEMF phase U • Jumper closed between pin 2 and pin 3: Hall sensor H1	Closed between pin 2 and pin 3
J11		Motor position feedback selector (see Section 4.2): • Jumper closed between pin 1 and pin 2: BEMF phase V • Jumper closed between pin 2 and pin 3: Hall sensor H2	Closed between pin 2 and pin 3
J12		Motor position feedback selector (see Section 4.2): • Jumper closed between pin 1 and pin 2: BEMF phase W • Jumper closed between pin 2 and pin 3: Hall sensor H3	Closed between pin 2 and pin 3
J13	CP	Allows to short the CP pin of the STDRIVE101 to GND, thus disabling the overcurrent protection (see Section 5.1).	Open (OC protection enabled)

Table 4. Power connectors description

Ref.	Pin Label	Description
CON1	VM	Main power supply (positive pole) of the power MOSFETs and the STDRIVE101. It ranges from 6 V to 75 V
	GND	Reference ground terminal (negative pole) of the main power supply.
CON2	U	Motor's phase U
	V	Motor's phase V
	W	Motor's phase W

Table 5. **EVALSTDRIVE101 test points**

Ref.	Label	Description
TP1	DT	Test point connected to the DT/MODE pin of the STDRIVE101
TP2	pGND	Power GND – GND reference of the power stage
TP3	pGND	Power GND – GND reference of the power stage
TP4	sGND	Signal GND – GND reference of the STDRIVE101, digital signals and Opamps
TP5	sGND	Signal GND – GND reference of the STDRIVE101, digital signals and Opamps
TP6	V_M	Voltage supply of the motor (V_M) and the STDRIVE101
TP7	REG12	Test point connected to the REG12 pin of the STDRIVE101; it is the output of the embedded linear regulator
TP8	nFAULT	Test point connected to the nFAULT pin of the STDRIVE101
TP9	VBUS	Feedback signal coming from a voltage divider connected to the motor voltage supply V_M
TP10	W	Test point connected to the phase W of the motor
TP11	V	Test point connected to the phase V of the motor
TP12	U	Test point connected to the phase U of the motor
TP13	VM	Voltage supply of the motor (V_M) and the STDRIVE101
TP14	pGND	Power GND – GND reference of the power stage
TP15	3V3	3.3 V digital voltage coming from the control board
TP16	ISNSG_U	Output of the opamp which amplifies the signal coming from the phase U shunt resistor
TP17	ISNSG_V	Output of the opamp which amplifies the signal coming from the phase V shunt resistor
TP18	ISNSG_W	Output of the opamp which amplifies the signal coming from the phase W shunt resistor
TP19	TEMP	Test point connected to the NTC resistor for the temperature sensing

3.1 Motor control connector

The motor control connector is used in many different ST evaluation boards embedding a STM32 microcontroller. Therefore, the EVALSTDRIVE101 can be controlled with different MCUs, allowing to choose the most suitable one for the target application. The **MC connector** on the EVALSTDRIVE101 can be wired to the MCU board using a 34 pole 1,27 mm pitch flat cable. The pinout description of the MC connector is reported in Table 6 .

Table 6. **MC connector (J4) pinout description**

Pin.	Net Label	Description
1	nFAULT	nFAULT open-drain pin of the STDRIVE101; it is used to signal a FAULT condition to the MCU (see Section 5.5).
2	GND	GND reference
3	IN_U	STDRIVE101 digital input signal (**IN1/INH1**). It drives the HS driver of the phase U or the status of the phase U half-bridge, according to the selected input strategy (see Section 5.4).
4	GND	GND reference
5	EN_U	STDRIVE101 digital input signal (**EN1/INL1**). It drives the LS driver of the phase U or it enables the phase U half-bridge, according to the selected input strategy (see Section 5.4).
6	GND	GND reference
7	IN_V	STDRIVE101 digital input signal (**IN2/INH2**). It drives the HS driver of the phase V or the status of the phase V half-bridge, according to the selected input strategy (see Section 5.4).
8	GND	GND reference

Pin.	Net Label	Description
9	EN_V	STDRIVE101 digital input signal (**EN2/INL2**). It drives the LS driver of the phase V or it enables the phase V half-bridge, according to the selected input strategy (see Section 5.4).
10	GND	GND reference
11	IN_W	STDRIVE101 digital input signal (**IN3/INH3**). It drives the HS driver of the phase W or the status of the phase W half-bridge, according to the selected input strategy (see Section 5.4).
12	GND	GND reference
13	EN_W	STDRIVE101 digital input signal (**EN3/INL3**). It drives the LS driver of the phase W or it enables the phase W half-bridge, according to the selected input strategy (see Section 5.4).
14	VBUS	Feedback signal coming from a voltage divider connected to the motor voltage supply V_M (see Section 4.4)
15	IS1	Current sensing signal related to motor's phase U (see Section 4.1)
16	GND	GND reference
17	IS2	Current sensing signal related to motor's phase V (see Section 4.1)
18	GND	GND reference
19	IS3	Current sensing signal related to motor's phase W (see Section 4.1)
20	GND	GND reference
21	GPIO-BEMF	Digital signal enabling the resistor divider for BEMF reading (see Section 4.2.2)
22	GND	GND reference
23	--	Not connected
24	GND	GND reference
25	+5V	+5V auxiliary supply coming from the MCU board; it is used for the position sensors supply, if selected (see Section 4.2)
26	T_OUT	Temperature reference voltage coming from the NTC resistor (see Section 4.3)
27	--	Not connected
28	VDD	V_{DD} voltage (3.3 V) coming from the MCU board; it is the supply of the MCU. It is also used to supply the opamps and as a digital reference level
29	--	Not connected
30	GND	GND reference
31	H1-BEMF1	Position feedback signal for phase U (see Section 4.2.1)
32	GND	GND reference
33	H2-BEMF2	Position feedback signal for phase V (see Section 4.2.1)
34	H3-BEMF3	Position feedback signal for phase W (see Section 4.2.1)

3.2 Getting started

Using the default configuration described above, it is possible to develop a project for a three-phase brushless motor. Table 7 summarizes the maximum ratings of the EVAL STDRIVE101. To run the motor follows the points below:

- Connect a power supply (voltage between 6 V and 75 V) to CON1 taking care to connect the positive pole to VM pin and the negative one to GND pin (see Figure 1)
- Connect the three-phase brushless motor to CON2 taking care of the motor phase sequence
- Select the supply of the Hall sensors using J8 and connect the Hall sensors and their supply to J9 (disregard this point if the application does not require Hall sensors)
- Connect the motor control connector J4 to a compatible control board (e.g. the X-NUCLEO-IHM09M1 adapter together with a NUCLEO-F303RE)
- Download the target firmware in the MCU

- Power up the voltage supply connected to CON1 and then supply the control board.

Note: ***The 3.3 V digital voltage present on the EVALSTDRIVE101 is provided by the control board and usually corresponds to the supply of the MCU.***

Table 7. EVALSTDRIVE101 Operative conditions

Parameter		Value
Supply voltage	Nominal	From 6 V to 75 V
Maximum phase current	Continuous(1)	20 A_{rms}
	Peak (OC protection enabled – J13 open)	35 A
	Peak (OC protection disabled – J13 closed)	45 A

1. *Actual maximum current could be limited by power dissipation*

Note: ***For a preliminary evaluation of the STDRIVE101, it is possible to connect a generic MCU board to a reduced subset of the J4 – MC connector pins:***

- The six input digital lines of the device (pins 3, 5, 7, 9, 11, 13)
- The three feedback signal of the phase currents (pins 15, 17, 19)
- Provide the 3.3 V supply on pin 28

In addition to these pins, pin 1 for FAULT monitoring and pin 14 for V_M monitoring can be used.

3.3 Mounting the heatsink

The EVALSTDRIVE101 comes with a custom heatsink and a 75 x 75 mm thermal interposer, which enables the coupling between the copper on the bottom layer and the heatsink.

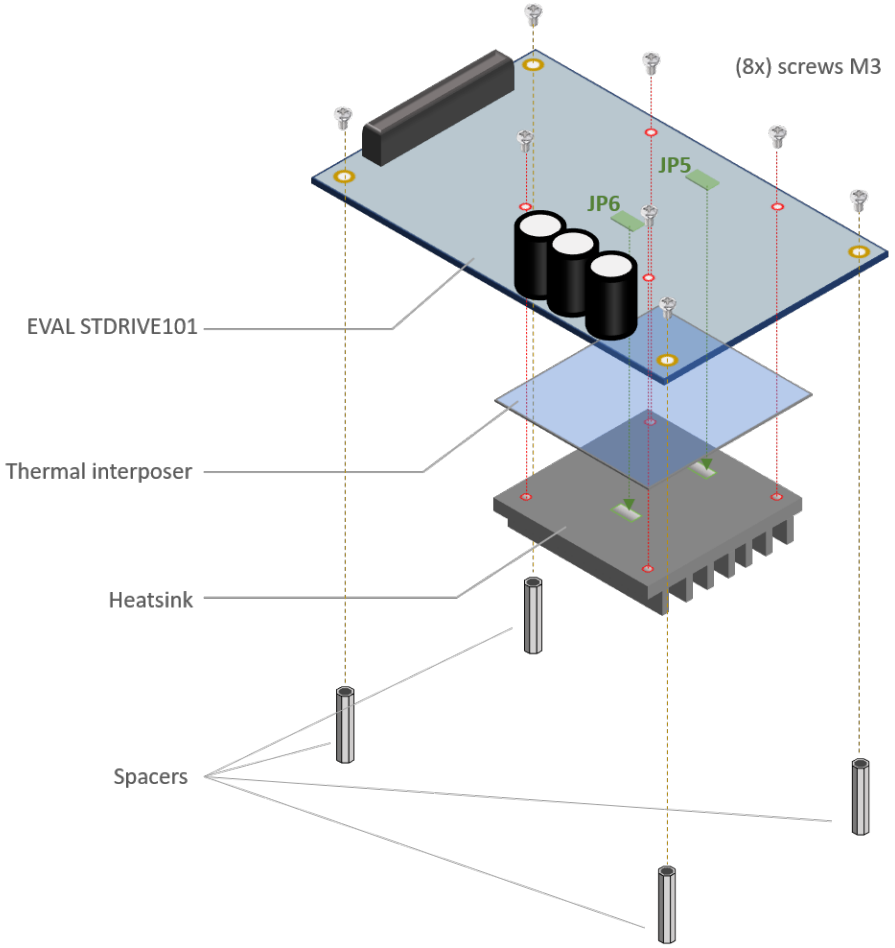
To increase the power dissipation of the EVALSTDRIVE101, the provided heatsink can be screwed on the bottom of the board. The heatsink covers the entire area of the power stage and the dissipation area of the STDRIVE101. The power solder bridges JP5 and JP6 are covered by the heatsink, so they must be soldered (if needed) before mounting the heatsink. Since the soldering can introduce an additional thickness, the heatsink is engraved with two carvings in correspondence of each solder contact. For a correct mounting of the heatsink, follow the steps below:

- Solder the JP5 and JP6 in case of single shunt configuration (see Section 4.1.1)
- Remove the protective film from both sides of the thermal interposer
- Stack up the board, the thermal interposed and the heatsink, taking care to align the threaded holes of the heatsink with the holes on the EVALSTDRIVE101. Concurrently, align the two carvings on the surface of the heatsink to JP5 and JP6 solder contacts
- Tighten the four screws in order to fix the heatsink to the EVALSTDRIVE101
- Mount the spacers at the four corners of the EVALSTDRIVE101

At the end of the process, ensure that:

- there are no gaps between the heatsink and the bottom layer of the board
- the PCB edge does not result in bending, due to excessive screws tightening

Figure 8. **Heatsink stack-up diagram**



4 Board and functional blocks description

The EVALSTDRIVE101 is an evaluation board based on the STDRIVE101, a three-phase gate driver. The power stage is based on the N-channel STL110N10F7 power MOSFETs in a 5x6 powerFLAT package. The digital control signals and the feedback signals are routed on the motor control connector, compatible with several STM32 microcontrollers boards.

The board can be configured in single shunt and three-shunt and it can support FOC and six-step algorithms in both configurations. The Operational amplifiers present on the EVALSTDRIVE101 allow a differential reading of the shunt resistors; the amplification and conditioning of the signals allow very precise measurement of the current flowing in the motor phases.

The Hall sensors connector and the phase sensing network present onboard enable the motor position feedback, allowing to implement both sensor and sensorless algorithms for motion control.

The EVALSTDRIVE101 is suitable for a full evaluation of the STDRIVE101 and its features, including the embedded comparator for overcurrent protection and the VDS monitoring protection.

4.1 Current sensing

4.1.1 Shunt resistor configuration

The EVALSTDRIVE101 can be used in both three-shunt or single shunt configurations. By default, the board is configured in three-shunt configuration. Every phase has up to three footprints for 2512 SMD shunt resistors. Just two 10 mΩ resistors are mounted enabling an equivalent 5 mΩ for each phase; the unmounted resistor enables more flexibility in case of shunt value modification. The advantages to having more resistors in parallel is the power dissipation improvement and a higher flexibility in case of shunt's value modification.

It is possible to select which signal for current sensing can be fed on the MC connector (J4) and thus to the MCU: the raw signal of the sense resistor or the latter amplified and filtred. The selection can be done using:

- J5 for the current sensing of the phase U
- J6 for the current sensing of the phase V
- J7 for the current sensing of the phase W

Closing with a jumper pin 1 and pin 2 of the connector (default configuration) sends the amplified signal to the MC connector; closing pin 2 and pin 3 sends the raw signal of the sense resistor to the MCU board. Using the default configuration (amplification on board) improves the performance because of noise and common mode rejection.

Table 8. Default configuration of each set of shunt resistors

	Phase U	Phase V	Phase W
Mounted shunt resistors	R23, R24	R25, R26	R27, R28
Not mounted shunt resistor	R73	R74	R75
Sensing opamp stage	U2	U3	U4
Amplified signal test point	TP16	TP17	TP18
Amplified/raw signal selector jumper	J5	J6	J7
MC connector label	IS1 (J4 - pin 15)	IS2 (J4 - pin 17)	IS3 (J4 - pin 19)

It is possible to change the EVALSTDRIVE101 configuration from three-shunt to single shunt by closing the JP5 and JP6 solder contacts on the bottom layer of the board. The three sources of the LS power MOSFETs are tied together, thus enabling the single shunt configuration. Since the entire load current flows through JP5 and JP6, the soldering must cover the whole length to minimize the contact impedance.

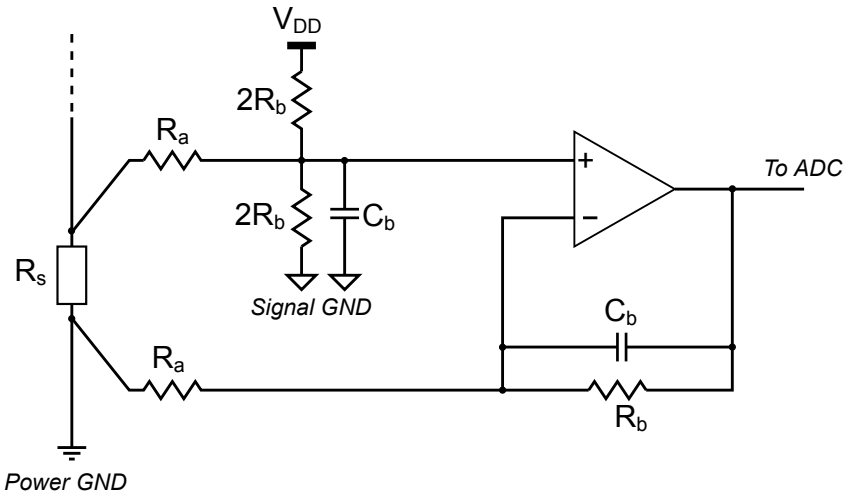
Note: ***The JP5 and JP6 soldering must be done before mounting the heatsink; see section Section 3.3 for further details.***

When JP5 and JP6 are closed, all the shunt resistors present on the board result in parallel, decreasing the total resistive value. To keep the default shunt value at 5 mΩ, the shunt resistors related to phase U and W must be removed. To have more symmetry in the layout of the current paths, it is suggested to use the phase V shunt resistors as a sensing element for the current of the power stage. Concurrently, use the U3 amplification circuitry (related to phase V), to sense and acquire the current. Moreover, the U3 opamp allows to double the gain if needed (further information can be found in the Section 4.1.2).

4.1.2 Operational amplifier network

The EVALSTDRIVE101 embeds three operational amplifiers to amplify the signals coming from the shunt resistors. The generic schematic is shown in Figure 9: it is also valid for opamp U3 (phase V amplifying network), since JP7 and JP8 are closed by default.

Figure 9. Opamp network schematic



The differential topology allows to reject the common mode on the shunt resistor thus improving the readout precision. The resistor net on the non-inverting input allows to shift the signal to read both positive and negative currents. When the current in the corresponding shunt resistor is zero, the output of the operational amplifier is nominally $V_{DD}/2$ (about 1.65 V). Therefore, both positive and negative currents can be sensed in this topology, as required by the FOC algorithm.

The current I_{ph} flowing in the sense resistor generates a voltage $V_s = R_s \cdot I_{ph}$ that is amplified by the opamp network. The DC gain is equal to:

Equation 1

$$G = \frac{R_b}{R_a} = \frac{10\ k\Omega}{1.54\ k\Omega} \approx 6.5 \quad (1)$$

The maximum measurable current is determined by the dynamic of the opamp's output:

Equation 2

$$I_{meas} \cdot\ R_S \cdot G < \frac{V_{DD}}{2} \Rightarrow I_{max} = \frac{V_{DD}}{2R_S \cdot G} \approx 50\ A \quad (2)$$

The capacitors C_b introduce a filter to reduce the noise with a cut-off frequency equal to:

Equation 3

$$f_T = \frac{1}{2\pi \cdot\ R_b \cdot C_b} = \frac{1}{2\pi \cdot 10\ k\Omega \cdot 22\ pF} \approx 720\ kHz \quad (3)$$

The capacitor on the non-inverting input must have the same value of the feedback capacitor to match the impedance of the non-inverting gain and the inverting gain.

Due to very small shunt values, the signals must be taken as close as possible to the shunt's terminals. Table 9 lists the correspondence between the generic schematic in Figure 9 and the EVALSTDRIVE101 components' references.

Table 9. EVALSTDRIVE101 components in the opamp network

	Value	U2 Opamp phase U	U3 Opamp Phase V	U4 Opamp Phase W
R_a	1.54 kΩ	R52, R56	R58, R62	R67, R70
R_b	10 kΩ	R53	R60	R68
$2R_b$	20 kΩ	R54, R57	R61, R64	R69, R72
C_b	22 pF	C22, C26	C27, C28	C31, C32

Values of the components can be changed in order to change gain and bandwidth of the amplification stage, but the relations between components must be kept the same. For example, all the resistors indicated as R_a must always have the same value as well as $2R_b$ resistors having to be always twice than the R_b resistors.

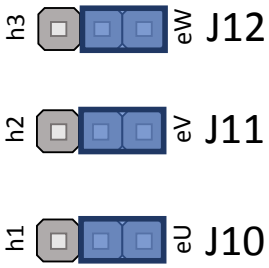
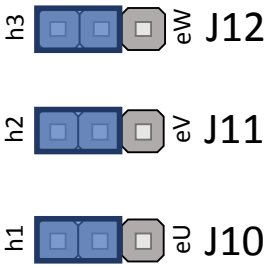
Note: ***Changing the gain of the opamps impacts on the overcurrent protection threshold. Refer to Section 5.1 for more information.***

In case of single shunt configuration, where just positive current sensing is required (e.g. six-step driving), it is possible to double the gain removing the solder contacts JP7 and JP8. Opening JP7 increases the total value of the feedback resistor, that is given by the sum of R59 and R60; opening JP8 disconnects the R61 resistor, removing the biasing at V_{DD} and matching the impedance of the non-inverting and the inverting inputs of the opamp. In this condition the bandwidth is halved. In case of zero current in the shunt resistor the output of the opamp is equal to 0 V: negative signals cannot be measured. This modification can be done only on the opamp U3 connected to the phase V. For this reason, it is recommended to use this opamp in case of single shunt measurement: the shunt resistor mounted in single shunt configuration should be mounted on R25, R26 and R74 footprints.

4.2 Motor position feedback

The position feedback signals are sent to the MCU via the MC connector J4: pin 31, pin 33 and pin 34 are related respectively to phase U, phase V and phase W. It is possible to select which are the signals to be used for the position feedback, whether the BEMF signals or the digital Hall/encoder sensors signals. The selection is done through J10, J11 and J12. Setting the jumpers between pin 2 and 1 (towards the labels “eU”, “eW” and “eW”), the BEMF are used as position feedback signals. Setting the jumpers between pin 2 and pin 3 (towards the labels “h1”, “h2” and “h3”) the Hall sensors signals are used instead.

Table 10. **Jumper configuration for position feedback selection**

	BEMF as position feedback signals	Hall sensor as position feedback signals
J10	jumper towards “eU” label	jumper towards “h1” label
J11	jumper towards “eV” label	jumper towards “h2” label
J12	jumper towards “eW” label	jumper towards “h3” label
Diagram		

4.2.1 Hall/encoder sensor connector

The sensors can be connected to the EVALSTDRIVE101 through the J9 connector as reported in Table 11.

Table 11. **Hall/encoder connector (J9)**

Label	Pin	Description
A+/H1	1	Hall sensor 1/encoder out A+
B+/H2	2	Hall sensor 2/encoder out B+
Z+/H3	3	Hall sensor 3/encoder zero feedback
Vhall	4	Sensor supply voltage
GND	5	Ground

For sensors requiring an external pull-up, three 10 kΩ resistors are already mounted on the output lines and connected to the V_{DD} voltage. Each line is filtered by an RC low-pass filter given by R37, R38, R39 and C19, C20 and C21. On the same lines, footprints for pull-down resistors are also available (R40, R41 and R42).

The jumper J8 selects the power supply for the sensor supply voltage:

- Jumper between the pin 1 and pin 2: sensors powered by (VDD = 3.3 V)
- Jumper between the pin 2 and pin 3: sensors powered by 5 V

Both supplies are provided externally and brought on board by the MC connector J4.

4.2.2 BEMF sensing network

The three voltages of the motor’s phases are sensed through a passive network to acquire the BEMF when one phase is in a high impedance state (six-step algorithm). The purpose of the acquisition is to detect the BEMF zero-crossing in order to know the rotor position.

Since the motor’s phases can reach a voltage up to 75 V, an attenuation network is implemented; setting the digital line “GPIO_BEMF” to 0 V, the resistor divider is enabled (attenuation factor about 0.07). This digital line can be synchronized with the PWM driving the motor phases or it can be statically set to 0 V according to the algorithm used. Clamping diodes are present to protect the MCU from overshoots above V_{DD} (D7, D10, D13) and undershoots below GND (D9, D12, D15).

4.3 Temperature sensor

The NTC resistor is placed close to the half-bridge of the phase V, in the center of the board. This is supposed to be the hottest point when the board is operating at high currents. A voltage proportional to the temperature is generated on the T_OUT net in the middle of the resistors' divider given by the NTC (R29) and R30. The signal is filtered by C39 and sent to pin 26 of MC connector J4. The NTC resistance decreases when the temperature increases with a non-linear relation (Figure 10). R30 is sized in order to get a linear behavior in the temperature range between 50°C and 120°C, as shown in Figure 11. The relation to find the temperature starting from the voltage readout is:

Equation 4

$$T[°C] = 45.7 \cdot V_{TP19}[V] + 23.6 \quad (4)$$

Figure 10. NTC resistance value with respect to temperature

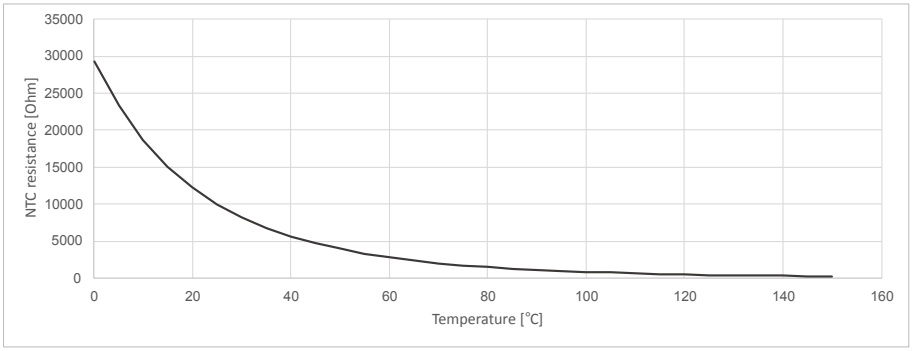
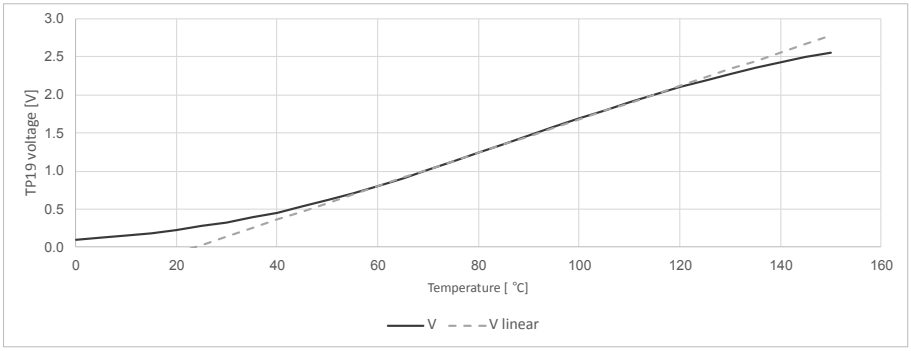


Figure 11. Voltage on TP19/T_OUT net with respect to temperature



4.4 Bus voltage monitoring

The bus voltage V_M cannot be directly acquired by the MCU since it ranges from 6 V to 75 V. Therefore, it is scaled down by R9 and R10, with an attenuation factor of 0.035. The signal is then filtered by C10 and sent to pin 14 of MC connector J4.

5 STDRIVE101 features description

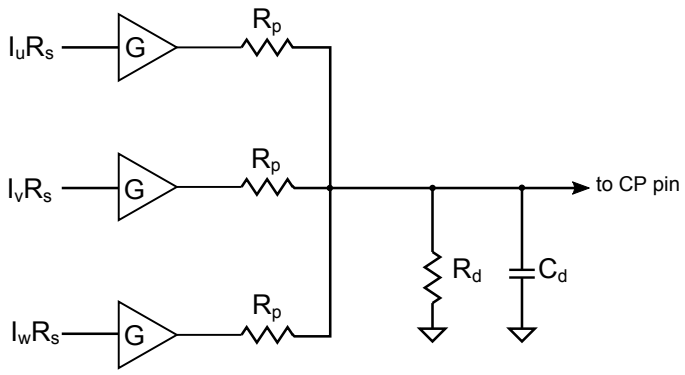
5.1 Overcurrent comparator

The STDRIVE101 integrates a comparator, which disables the power stage whenever the voltage on its input (CP pin) exceeds the internal threshold V_{REF}, about 0.5 V. The values of the currents in each phase are acquired and combined through a network of components: the resulting signal is connected to CP. The values of the components are chosen to obtain the desired current limit.

Note: ***The overcurrent protection can be disabled shorting the CP pin to GND, closing with a jumper the connector J13.***

In the default configuration the phase currents are monitored by the opamps; R55, R63 and R71 connect each opamp output to a common node and R65 acts as a voltage divider to adapt the signal to the input range of the CP pin of the STDRIVE101. Referring to Figure 12, which provides a simplified diagram of the overcurrent network, R55, R63 and R71 must have the same value represented as R_p; R65 and C29 are represented respectively as R_d and C_d.

Figure 12. Simplified diagram of the overcurrent network for three-shunt configuration



The value of the resistors R_p and R_d can be calculated according to the following formula, for a target value of overcurrent threshold (I_{OC}):

Equation 5

$$\frac{R_d}{R_p + 3R_d} = \frac{V_{REF}}{I_{OC} \cdot R_S \cdot G + \frac{3}{2}V_{DD}} \quad (5)$$

It must be considered that the gain G of the opamp, the sense resistor R_S and the overcurrent value I_{OC} must be chosen to avoid the opamp saturation:

Equation 6

$$I_{OC} \cdot R_S \cdot G < \frac{V_{DD}}{2} \quad (6)$$

The low-pass filtering introduced by C_d gives the following cut-off frequency:

Equation 7

$$f_{T,OC} = \frac{1}{2\pi C_d \cdot \frac{R_p \cdot R_d}{R_p + 3R_d}} \quad (7)$$

The default values of the EVALSTDRIVE101 are R_p = 10 kΩ, R_d = 1.1 kΩ and Cd = 3.3 nF leading to an overcurrent value I_{OC} = 33.7 A and a cut-off frequency $f_{T,OC}$ = 58 kHz. The delay introduced by the low-pass filtering increases the response time and thus the actual dynamic overcurrent threshold, with respect to the static value I_{OC} used for the calculation of Equation 5.

In case of single shunt configuration (see Section 4.1.1), Equation 5 and Equation 7 are no longer valid. A single opamp can be used to read the shunt resistor voltage, so R55 and R71 should be disconnected. The value of R63, R65 and C29 have to be modified in order to get the desired values of overcurrent threshold and bandwidth of the filter.

Equation 8

(8)

$$\frac{R65}{R63+R65} = \frac{V_{REF}}{I_{OC}\cdot R_S \cdot G + \frac{V_{DD}}{2}}\Bigg|_{R55,\,R71\ removed}$$

Equation 9

(9)

$$f_{T,OC} = \frac{1}{2\pi C_d \cdot (R63 \parallel R65)}\Big|_{R55,\,R71\ removed}$$

According to Equation 8 and Equation 9, the same values of overcurrent threshold and cut-off frequency of the previous case (three-shunt), i.e. I_{OC} = 33.7 A, and $f_{T,OC}$ = 58 kHz, are obtained using R65 = 2.2 kΩ , C29 = 1.5 nF, R63 unchanged (10 kΩ) and removing R55 and R71.

5.1.1 OC comparator alternative network

An alternative readout network can be used to read the signal: it is composed by R76, R77, R78 and R79. This net uses the raw signal coming from the sense resistors, so the OC threshold does not depend on the gain G of the opamp.

Note: ***When using this alternative network, the resistors R55, R63, R71, and R65 must be disconnected, while C29 or C30 footprint can be used to add some filtering against noise.***

In the three-shunt topology R76, R77, and R78 must have the same value. In the single shunt topology only R77 must be mounted, while R76 and R78 must be disconnected. The R79 allows to adjust the overcurrent threshold, since the internal V_{REF} has a fixed value.

5.2 VDS monitoring protection

The STDRIVE101 embeds a circuitry which measures the voltage between the drain and the source of each MOSFET (V_{DS}) and compares it with a specified threshold. When the MOSFET is turned on and its V_{DS} is greater than the threshold, the anomalous condition is detected and the protection is triggered after a deglitch time. The threshold is set on the SCREF pin of the STDRIVE101, through the resistors divider given by R2 and R4: it is approximately 1.03 V.

Note: ***The drop on the LS MOSFETs is measured between their drain and GND, so the drop on the respective shunt resistor contributes to the measure. For further information refer to STDRIVE101 datasheet.***

The VDS monitoring protection can be disabled closing with a jumper the pins of J1: the 3.3 V (VDD) is provided on SCREF pin of the STDRIVE101.

5.3 Embedded 12 V linear regulator

The STDRIVE101 embeds a linear regulator which supplies the gate drivers. The voltage generated by the linear regulator is available on the REG12 pin and the test point TP7 and it can be also used to supply small external loads.

In case the supply V_M of the power MOSFETs is less than 12 V, the output of the linear regulator can be shorted to V_M by closing with a jumper the connector J3.

Warning:

When J3 is closed, the voltage supply V_M provided on the CON1 must be less than 15 V, otherwise the STDRIVE101 undergoes permanent damage.

5.4 Working Mode selection

The STDRIVE101 has two input strategies (Table 12) which can be selected with a jumper connected on J2. For further information, refer to the STDRIVE101 datasheet.

Table 12. J2 status and related input strategy

J2 status	DT/MODE pin	Input strategy	Description
Open	Connected to R6 pull down	ENx/INx	The half-bridge “x” is enabled or disabled by ENx signal and its status is determined by INx signal
Closed	Connected to GND	INHx/INLx	The status of each driver is determined by the status of its input signal: INHx for the HS MOSFET and INLx for the LS MOSFET

Using the ENx/INx input mode, the deadtime is set by R6; the default 51 kΩ resistor gives a deadtime approximately around 570 ns.

5.5 Fault monitoring

A red LED (LED1) is present and it is activated by the nFAULT pin. When a protection of the STDRIVE101 is triggered (overcurrent, VDS monitoring, UVLO or overtemperature), the internal open drain MOSFET of the nFAULT pin is turned on, turning on the LED as well. The pin status can be read also on the TP8 test point, pulled up by the R8 resistor.

Revision history

Table 13. **Document revision history**

Date	Version	Changes
26-Oct-2020	1	Initial release.

Contents

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