



Gate Drive Evaluation Platform (GDEV) LF-SiC-EVB-GDEV1

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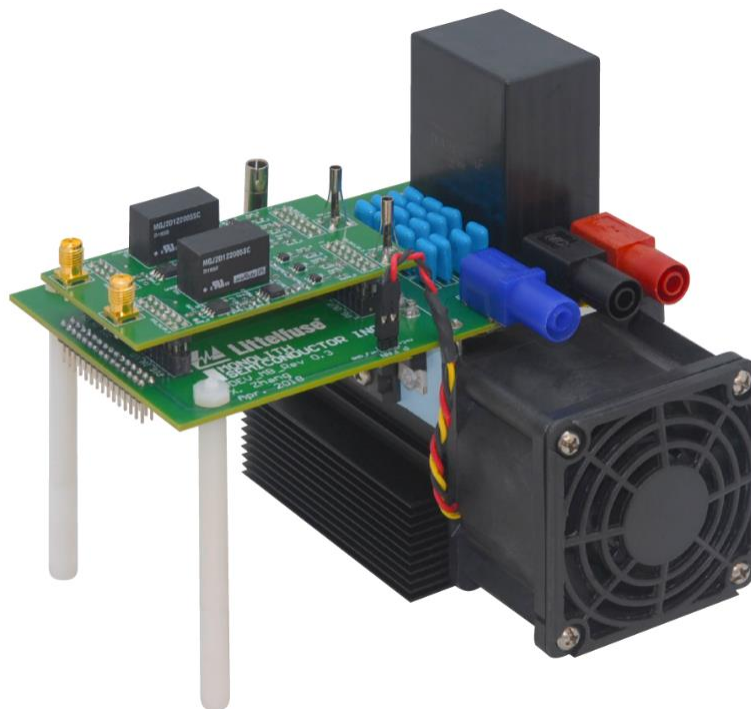
2. Design Summary

2.1. Objectives

The Gate Drive Evaluation Platform from Littelfuse enables users to:

- Evaluate continuous operation of SiC power MOSFETs and diodes under rated voltage and rated current, delivering real power to the load
- Analyze system-level impacts associated with SiC-based designs
 - Efficiency improvements
 - EMI emissions
 - Passive components (size, weight, cost)
- Compare the performance of different gate driver solutions under well-defined and optimized test conditions
- Test gate driving circuits under continuous working conditions to evaluate gate driver thermal performance and EMI immunity

The gate driver evaluation platform (GDEV) is an evaluation kit that has been designed to demonstrate the continuous operation of SiC power MOSFETs and diodes in a half bridge configuration. It provides a set of well-defined test conditions and quick-connection functionality to evaluate and compare the performance of different driving board designs with different driver ICs. It also features a full thermal solution that allows for the continuous operation of the power devices under high voltage and high current with real power delivery.



2.2. Design Reference Files

For more information about this evaluation kit, including design files, visit the GDEV webpage at:

- [Littelfuse.com/GDEV](https://www.littelfuse.com/GDEV)

2.3. Contact Information

To purchase a Gate Drive Evaluation Kit, visit:

- Littelfuse.com: Part No. LF-SIC-EVB-GDEV1
- Mouser.com: Part No. 576-EVAL-GDEP-01
- Digi-Key.com: Part No. 238-LF-SIC-EVB-GDEV1-ND

For technical details about the Gate Drive Evaluation Platform, contact the Littelfuse SiC Application Support team:

- powersemisupport@littelfuse.com

3. Introduction

The Gate Drive Evaluation Platform (GDEV) was designed to demonstrate the continuous operation of Littelfuse SiC power MOSFETs and diodes in a half-bridge configuration. In addition, it provides a well-defined testing environment for evaluating and comparing the performance of various driving board designs, as well as driver ICs. A full thermal management solution – via an integrated heatsink – allows for continuous operation of the power devices under rated voltage and current conditions. The GDEV can be used to:

- Evaluate continuous operation of SiC power MOSFETs and diodes under rated voltage and rated current, delivering real power to the load
- Analyze system-level impacts associated with SiC-based designs
 - Efficiency improvements
 - EMI emissions
 - Passive components (size, weight, cost)
- Compare the performance of different gate driver solutions under well-defined and optimized test conditions
- Test gate driving circuits under continuous working conditions to evaluate gate driver thermal performance and EMI immunity

The GDEV system consists of a motherboard that gate driver module boards can be plugged into quickly and easily. The modular gate driver boards and simplified interface strategy were chosen to optimize the functionality of this platform. This application note details the GDEV system architecture, presents several gate driver IC options and their technology characteristics, and provides an example of using the GDEV to evaluate the performance of SiC power MOSFETs and various gate driver ICs under continuous switching conditions.

Table 1. GDEV Mother Board Electrical Specifications

Parameter	Typical Value	Maximum Rating	Units
Input DC Link Voltage	800	900	V
Input Control Voltage	12	13.2	V
Input Cooling Fan Voltage	24	26.2	V
Ambient Temperature	25	45	°C

Note: Recommended maximum output power: 5 kW with 800 V input, 400 V output, 100 kHz f_{sw} , and provided cooling fan

Table 2. High Current Gate Diver

Parameter	Typical Value	Maximum Rating	Units
Input Control Voltage	12	13.2	V
Input Logic Voltage	3.3	5	V
Ambient Temperature	25	45	°C

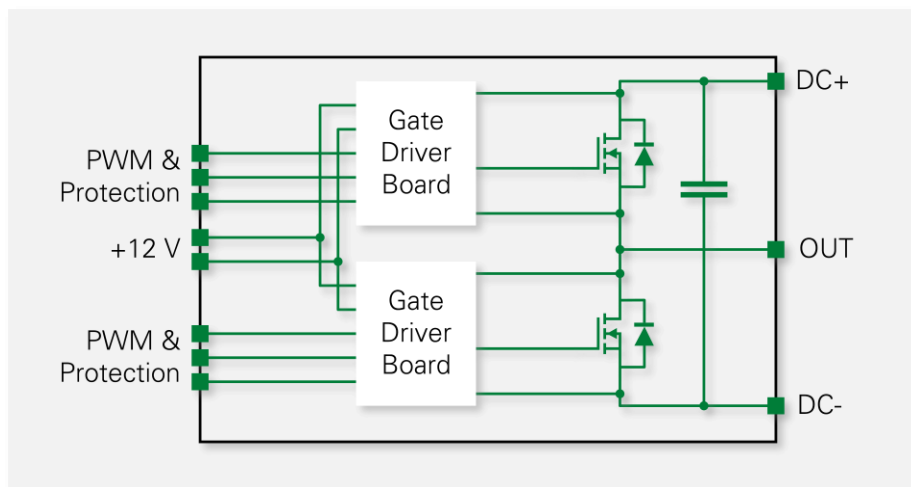
Table 3. Integrated Gate Diver with Protection Functions

Parameter	Typical Value	Maximum Rating	Units
Input Control Voltage	12	13.2	V
Input Logic Voltage	3.3	5	V
Ambient Temperature	25	45	°C

4. Gate Driver Evaluation Platform (GDEV) – Motherboard

The GDEV leverages a half-bridge configuration with gate driver module connections for both top and bottom position devices. It performs as a power stage reference design that allows users to test the performance of SiC MOSFETs and diodes under continuous switching conditions at high voltage and high current levels, delivering real power to the load. It also provides a well-defined and standardized testing environment for evaluating and comparing the performance of different driving board designs with different driver ICs. Figure 1 is a block diagram schematic of the gate driver evaluation platform. The power stage features a half-bridge configuration with the option to use a SiC power MOSFET, SiC Schottky diode, or both in parallel for each switch position. The power loop PCB layout shown in Figure 2 is optimized to minimize loop inductance and coupling between the power and gate loops. A probe-tip adapter allows for accurate drain-source voltage measurements.

Figure 1. Gate Driver Evaluation Platform Circuit Diagram



The GDEV features a full thermal management solution – via an integrated heat sink – that allows for continuous switching operation of the power devices under high voltage and high current, delivering real power to the load. It also allows for the evaluation of the gate driver thermal performance and EMI susceptibility under high switching frequencies commonly associated with SiC devices. This platform can be used as a half-bridge power stage reference design to test the impact that SiC devices might have on system-level performance metrics such as efficiency, EMI emissions, or the size and weight of passive components.

Figure 2. GDEV PCB Layout

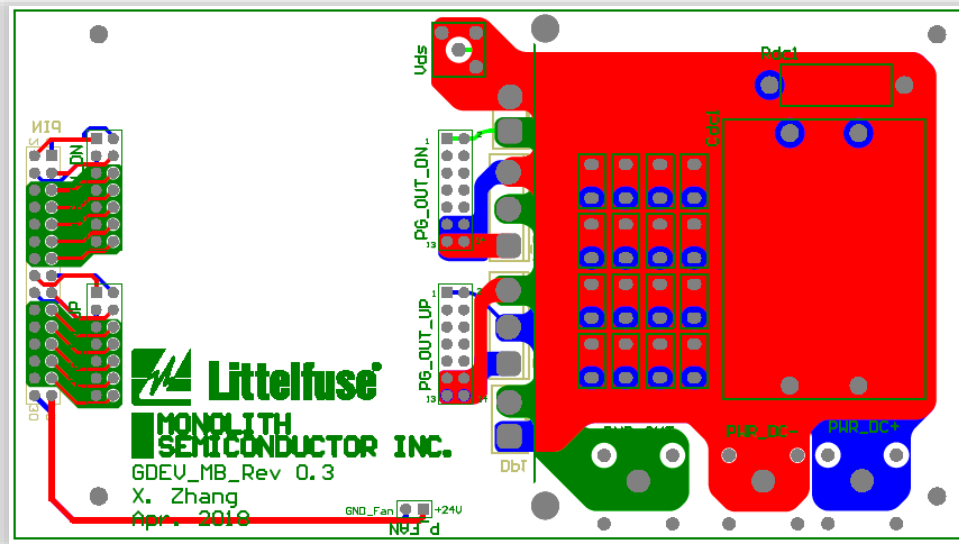
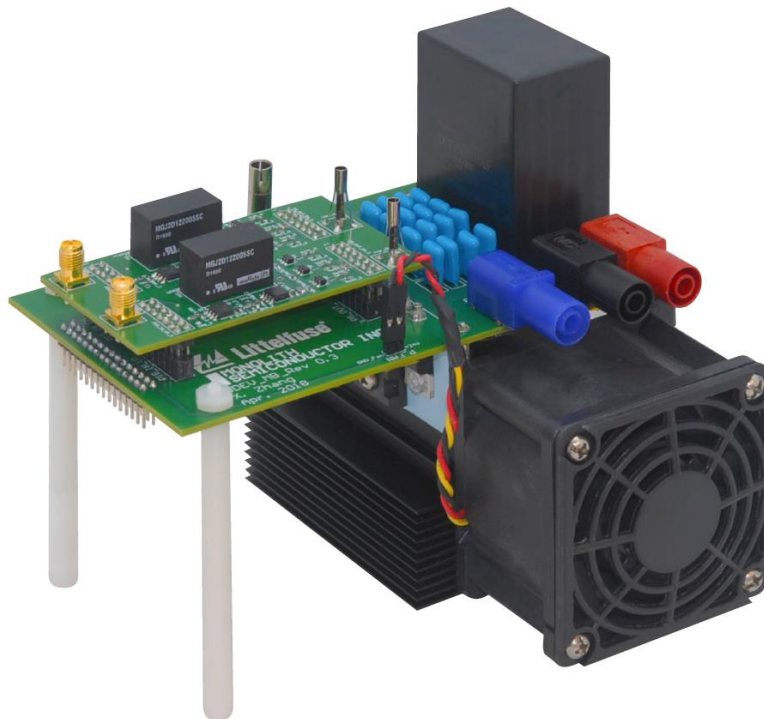


Figure 3 shows the GDEV hardware assembly with two gate driver boards, two SiC MOSFETs, two SiC diodes, and a full thermal management system.

Figure 3. GDEV Platform



4.1. Key Components and Signal Definitions

4.1.1. SiC MOSFETs and SiC Schottky Diodes

The power stage features a half-bridge configuration with the option of using SiC power MOSFETs in the 3L TO-247 package or SiC Schottky diodes in the 2L TO-220 package. In addition, a SiC MOSFET and a SiC diode may be used together in parallel for each switch position. The power loop is optimized to minimize loop inductance and coupling between the power and gate loops.

4.1.2. DC Link and Decoupling Capacitors

The GDEV platform includes a combination of capacitors that perform various functions. A single 10 μF film capacitor serves as a DC link capacitor to stabilize the DC link voltage during switching. Sixteen 0.22 μF ceramic capacitors are positioned very closely to the SiC devices and serve as the decoupling capacitors that provide energy during device switching. Together, the decoupling capacitors and DC link capacitor form a low-pass filter that filters the switching current on the DC bus. This reduces the impact of any parasitic inductance related to the wire connection between the DC source and the on-board DC bus of the test system.

4.1.3. Heatsink and Fan

The GDEV features a full thermal solution, including a heatsink and fan, for continuous operation of the gate driving circuit. A single heatsink from Wakefield-Vette [Part Number: OMNIUNI-18-75] is implemented such that all four possible power devices (two SiC MOSFETs + two SiC diodes) can be mounted to the heatsink for cooling purposes at the same time. A 24 V, 60mm x 60mm fan (65 CFM, Part Number: 9G0624G1011) provides additional forced air cooling.

4.1.4. Gate Driver Boards

In the GDEV system, the top and bottom switch positions in the half-bridge configuration each have individual gate driver accommodations. This allows users to evaluate top and bottom switch position driving characteristics independently. The modular gate driver boards are affixed to the motherboard both mechanically and electrically by way of 2x7 position header connectors. This allows for swapping different gate driver designs quickly and easily. Littelfuse has experimentally evaluated various gate driver ICs from a number of well-known gate driver IC suppliers. The results of these evaluations enable Littelfuse to make recommendations for gate driver ICs that pair well with Littelfuse SiC MOSFETs to satisfy various design constraints. Some of the observations are presented later in this document along with additional design details for the gate drive module components and PCBs.

4.1.5. Connectors and Measurement Points

Three high-voltage connection terminals are located on the GDEV motherboard: negative DC bus (DC-), positive DC bus (DC+), and the mid-point of the phase leg. The PWM signals and control power connections are provided via a 2x9 position header connector. A probe-tip adapter is provided for accurate measurement of the drain-source voltage of the bottom switch position's device. The gate-source voltage should be measured using the probe-tip adapter on the modular gate driver boards.

4.2. Connections and Signal Definitions

The signal and control power input connector is a 2x9 position header. Table 4 shows the pin-out definition of the header connector.

Table 4. Mother Board Input Signal/Power Connector

Pin	Definition	Pin	Definition
1	+12V_INPUT	2	GND_GDPS1
3	PWM1_IN	4	PWM1 GND
5	NC	6	GND_CTRL1
7	VCC_CTRL1	8	GND_CTRL1
9	RESET1	10	GND_CTRL1
11	FAULT1	12	GND_CTRL1
13	RDY1	14	GND_CTRL1
15	+12V_INPUT	16	GND_GDPS2
17	PWM1_IN	18	PWM2 GND
19	NC	20	GND_CTRL2
21	VCC_CTRL1	22	GND_CTRL2
23	RESET1	24	GND_CTRL2
25	FAULT1	26	GND_CTRL2
27	RDY1	28	GND_CTRL2
29	VCC_FAN IN	30	GND_FAN IN

Four 2x7 position header connectors provide easy connection and mechanical support for the gate driver modules. Two header connectors (PIG_IN_DN and PG_OUT_DN) are for the top switch position gate drive module; the other two header connectors (PIG_IN_UP and PG_OUT_UP) are for the bottom switch position gate drive module. Table 5 shows the pin-out definition for the input side for each of the gate drive modules (PIG_IN_DN and PIG_IN_UP).

Table 5. Gate Drive Module Input Signal Connector

Pin	Definition	Pin	Definition
1	GND_INPUT	2	+12V_INPUT
3	PWM1 GND	4	PWM1_IN
5	GND_CTRL	6	NC
7	GND_CTRL	8	VCC_CTRL
9	GND_CTRL	10	RESET
11	GND_CTRL	12	FAULT
13	GND_CTRL	14	RDY

Table 6 shows the pin-out definition for the output side for each of the gate drive modules (PIG_OUT_DN and PIG_OUT_UP).

Table 6. Gate Drive Module Output Signal Connector

Pin	Definition	Pin	Definition
1	Drain_MOSFET	2	Drain_MOSFET
3	NC	4	NC
5	NC	6	NC
7	NC	8	NC
9	NC	10	NC
11	Source_MOSFET	12	Source_MOSFET
13	Gate_MOSFET	14	Gate_MOSFET

Table 7 shows the pin-out definition for the cooling fan that is mounted to the motherboard heat sinks.

Table 7. Mother Board Fan Output Connector

Pin	Definition	Pin	Definition
1	VCC FAN OUT	2	GND FAN OUT

5. Gate Driver Evaluation Platform (GDEV) – Gate Driver Modules

The GDEV motherboard provides an optimized power stage design to evaluate SiC power MOSFETs in continuous operation. It also provides a well-defined test platform to evaluate and compare different gate driver designs in a standardized testing environment.

Littelfuse has taken the initiative to design and evaluate a number of gate drive modules using various off-the-shelf gate driver IC technologies (Table 8). The gate driver ICs chosen can be grouped into two primary categories:

- High current gate driver using separate isolation IC and gate driver IC** – These driver designs can provide high driving current, which can help to reduce device switching loss and driver IC temperature under high switching frequency conditions. It ensures the best switching performance of the SiC power MOSFET. Although it does not have integrated protection functions, users can add protection features using other discrete components.
- Integrated driver with protection functions** – These driver designs use integrated gate driver ICs that provide both driving and isolation functions. They can be further divided into categories based on the isolation technology: digital isolator-based gate driver or optocouplers-based gate driver. Often, these integrated driver ICs feature protection functionalities that include de-sat (overcurrent) protection, soft turn-off, active Miller clamping, UVLO, etc. These protection features can effectively protect SiC power MOSFETs under fault conditions. One limitation of the integrated driver design is that the driving current is typically less than 5 A, which might limit the SiC power MOSFET’s switching speed when a small external gate resistance is used; additionally, it might cause the driver IC to get hot under high switching frequency, especially for larger SiC power MOSFETs.

Table 8. Gate Driver Modules Designed and Evaluated by Littelfuse

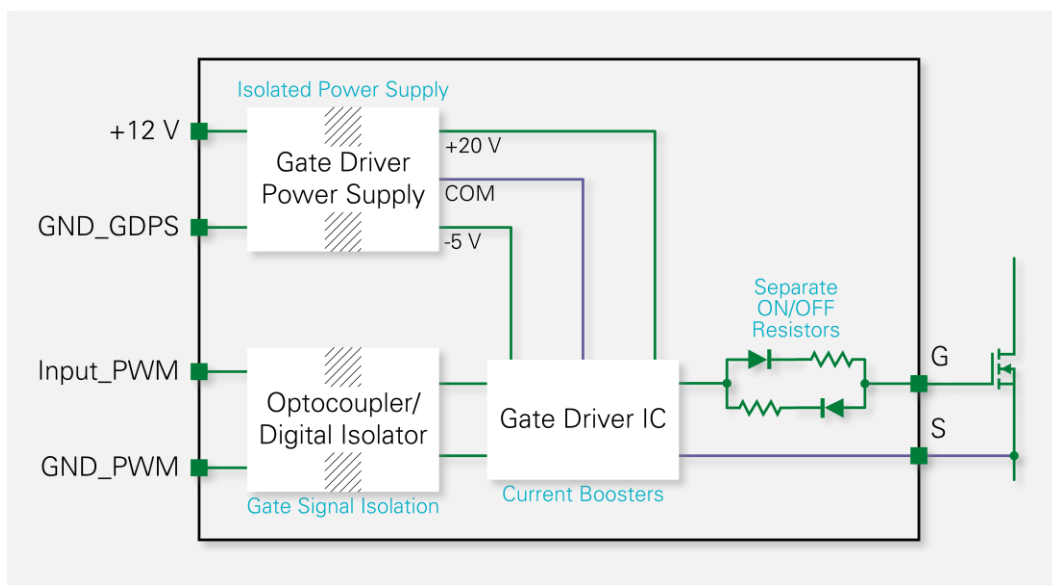
Part Number	Description
LSICRD-GD-ACPL332	Optocoupler-based gate driver with ACPL332J driver IC
LSICRD-GD-ACPL337	Optocoupler-based gate driver with ACPL-337J driver IC
LSICRD-GD-TLP5214	Optocoupler-based gate driver with TLP5214 driver IC
LSICRD-GD-ISO5852	Digital isolator-based gate driver with ISO5852S driver IC
LSICRD-GD-SI8285	Digital isolator-based gate driver with SI8285 driver IC
LSICRD-GD-IXDN609	High current gate driver with 9 A current driving capability
LSICRD-GD-IXDN614	High current gate driver with 14 A current driving capability

5.1. High Current Gate Driver Modules

5.1.1. Gate Driver Circuit Structure

Figure 4 is a block diagram schematic of the high current gate driver circuit (HCGD). It is an isolated gate driver that provides an appropriate driving voltage to a single MOSFET. It includes an isolated DC-DC power supply that converts a +12 V input DC voltage to +20 V and -5 V output DC voltages for the driving circuit. The gate signal isolation IC provides galvanic and high frequency isolation. The gate driver IC acts as a current booster to provide enough driving current to drive the SiC MOSFET. The ON/OFF resistors, when paired with an appropriately oriented diode in series, can control device turn-on and turn-off speed independently. The HCGD requires a +12 V input as the power supply to the gate driver circuit. The PWM input (Input_PWM/GND_PWM) is an emulated LED input driven by a current control signal. The typical PWM level is +3.3 V.

Figure 4. High Current Gate Driver Circuit Structure



This gate driver module design, shown in Figure 5, has two outputs pins (G and S), which connect to the gate and source of the SiC MOSFET respectively. A probe-tip adapter is included to ensure an accurate gate-source voltage measurement via a passive probe. The input and output connectors for this gate drive module design are 2x7 position header connectors with pinouts that match the signal interface of the GDEV motherboard.

Figure 5. LSICRD-GD-IXDN609 High Current Gate Driver with 9 A Current Driving Capability



(a) Top side view



(b) Bottom side view

5.1.2. Key Components and IC Selection

Three main components go into the high current gate driving circuit.

Gate Driver Power Supply

The gate driver isolated power supply provides correct driving voltages during turn-on and turn-off states. It should also provide good isolation for noise propagation. To simplify the design and ensure good system performance, a 5.2 kV DC isolated 2 W DC-DC converter [Part Number: MGJ2D122005SC] from Murata is used in each of the Littelfuse gate drive module designs. This DC-DC converter accepts a 12 V input voltage and produces +20/-5 V dual output voltages. The isolation capacitance from input side to output side is only 3.3 pF, which provides a good isolation barrier for gate driving circuits.

Gate Driver IC

The gate driver IC acts as a current boost stage that executes the switching action between positive and negative driving voltages during device switching transients. The gate driver IC should be able to provide/sink enough pulsed current to charge/discharge the power devices' gate quickly, to achieve low switching loss on power devices. Meanwhile, the gate driver IC should also have enough continuous current driving capability to provide adequate current and maintain a low driver IC temperature during continuous switching. To achieve high current driving capabilities, ensure low switching loss in the power MOSFET, and maintain good thermal performance during continuous switching at high frequency, a 9 A Low-Side Ultrafast MOSFET Driver from IXYS [Part Number: IXDN609] is used. The required current rating of the gate driver IC is highly dependent on the gate charge value of the power MOSFET it is driving and the external gate resistance value. IXYS also offers a 14 A Low-Side Ultrafast MOSFET Driver [Part Number: IXDN614] for higher current rating power MOSFETs or ultra-low external gate resistance applications.

Gate Signal Isolation IC

Due to the fast switching speed of SIC MOSFETs, high dv/dt exists in the system that generates high common mode current which propagates through the system. High common mode current can affect the voltage reference node in the control circuit and lead to faulty operation of the control circuit. The common mode current is determined by the dv/dt of the system and the propagation path impedance. To prevent excessive common mode current, a high isolation impedance is needed. Typically, the isolation capacitance of the gate signal isolation IC (from primary side to secondary side) is recommended to be less than 1 pF.

The two primary types of isolation ICs employ different isolation technologies: optocouplers and digital isolators. Digital isolators can be further divided by way of capacitive isolation and inductive isolation. In general, both optocouplers and digital isolators can provide adequate isolation for gate driving circuits. Each has its own merits and drawbacks. Optocouplers have been widely used for decades and their reliability is well established. With the electrical-to-optical-to-electrical single conversion theory, optocouplers offer physical isolation inside that might be needed to meet certain safety standards. The optocoupler is a current driving device, which makes the input signal less sensitive to EMI noise. Optocouplers usually have a lower data rate and larger pulse with distortion time when compared to digital isolators. Additionally, an optocoupler's performance might vary depending on driving voltage, temperature, and device age.

Conversely, the digital isolator is a relatively new technology and the IC parameters are typically better than an optocoupler's. Examples of these enhanced parameters include a higher transmission data rate, greater parameter stability over IC working conditions, and a smaller pulse width distortion time. One challenge with the digital isolators is the lack of physical isolation between the primary and secondary side. Additionally, most digital isolators require a voltage input signal, which might be more sensitive to EMI noise than a current signal. [1][2]

In general, both optocouplers and digital isolators can provide good gate drive circuitry isolation at both low and high switching frequencies. When selecting between optocouplers and digital isolators, compare these key parameters:

- **Isolation capacitance** – Because SiC MOSFETs switch within tens of nanoseconds, the isolator must maintain a high isolation impedance (up to hundreds of Megahertz) to mitigate common mode current propagation effects. Therefore, the isolation capacitance should be as small as possible. The isolation capacitance of digital isolators can be as low as 1 pF; the isolation capacitance of optocouplers can be as low as 0.6 pF.
- **Pulse width distortion time** – In half-bridge configurations, a deadtime is needed to avoid shoot-through failures. Excessive deadtime will create waveform distortion and generate low frequency noise, so it is preferable to use the minimum deadtime necessary. The minimum deadtime is typically determined by the larger number of either the switching speed of the devices or the propagation delays of the gate driver. The switching speed of SiC MOSFETs is typically tens of nanoseconds. The minimum deadtime must be designed for the worst case of driver IC propagation delays. In general, digital isolators have tighter propagation delay variations than optocouplers.
- **Common mode transient immunization (CMTI)** – Due to the high switching speed of SiC MOSFETs, there is high common mode noise propagation in the systems. The driver IC will subsequently be subjected to common mode voltage across both the primary and secondary sides. Therefore, it is recommended that the isolation IC be able to withstand high CMTI; however, it does not mean that the driver IC CMTI value must be equal with the maximum dv/dt in the circuit. The dv/dt generated in the power loop will be shared by the whole system and will not be focused on the isolation IC. Thus, it is advantageous for the IC to have a good CMTI value, but it must be considered together with other key parameters.

The 5 kV LED Emulator Input Gate Driver from Silicon Lab [Part Number: Si8261] was selected as the gate signal isolation IC to ensure an adequate isolation barrier with good resistance to temperature and aging, and with a tighter parameter distribution. The emulated LED input also provides a good differential input signal to improve noise immunity.

5.1.3. Gate Driving Loop Layout Design

In practical applications, PCB traces and ground copper planes will add parasitic capacitance and inductance to the circuit. These parasitics, shown in Figure 6, will be added to the package-related parasitics of the devices and will influence the device switching performance. The stray capacitance between gate and source of the devices will increase the Miller current and worsen the Miller effect. The gate-source stray capacitance will also increase the driving current requirement from the driver circuit. The stray inductance will increase the gate-source voltage overshoot and can lead to ringing during the switching transient. The maximum allowable gate voltage during a transient event is 5 V above the nominal driving voltage; thus, it is very important to keep the stray inductance as small as possible.

Figure 6. Gate Driver Circuitry Stray Inductance Sources

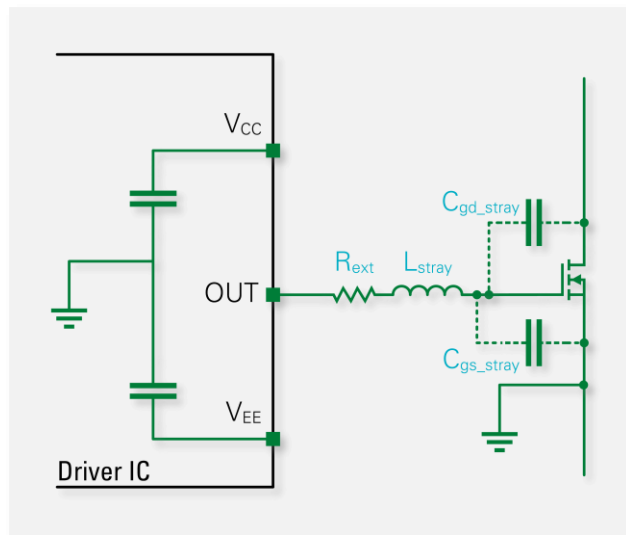
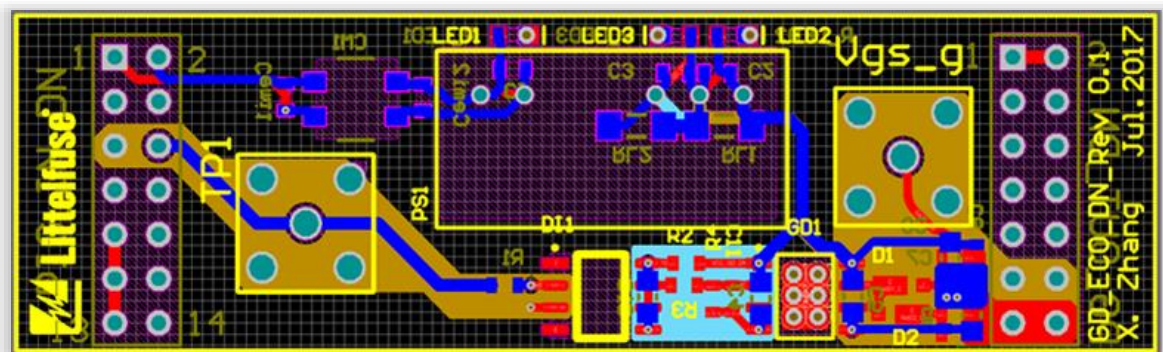


Figure 7 shows the PCB design details of the high current gate driver board. To reduce the PCB layout-related parasitic inductance and capacitance, the gate driving loop must be designed carefully and the trace routing must be optimized. Some good practice design guidelines are listed below.

Figure 7. High Current Gate Drive Module PCB Layout



Short Gate Path

Keeping the gate path as short as possible is recommended. The gate loop starts from the decoupling capacitor of the driver IC, includes the external gate resistor to the gate of the device, and returns to the decoupling capacitor via the source of the device. To minimize the gate loop distance, the driver IC, gate resistor, and decoupling capacitor should be placed as near to the gate of the device as possible.

Return Path Control

The gate loop return path should be routed directly below the gate trace to minimize the loop inductance.

Smaller C_{GD}

Larger C_{GD} will increase the current injected into the gate of the device and make the Miller effect worse. Minimizing the C_{GD} attributed to circuit layout by reducing the overlap area between gate-connected traces and drain-connected traces is recommended.

Use Ground Planes Cautiously

Ground planes provide a voltage reference and ensure the mirror current propagates optimally, but they can lead to problematic capacitive coupling. Using ground planes cautiously and only when necessary is recommended.

Decoupling Capacitor

Placing a decoupling capacitor as close to the driving IC as possible is recommended. The gate loop always starts from one polarity of the driver IC decoupling capacitor and ends at the other polarity. Placing the decoupling capacitor close to the driving IC can effectively reduce the gate current loop distance and thus the gate loop inductance. Because the decoupling capacitance provides all the transient gate switching current and gate charge needed, the decoupling capacitor should be large enough to minimize gate voltage changes during switching transient.

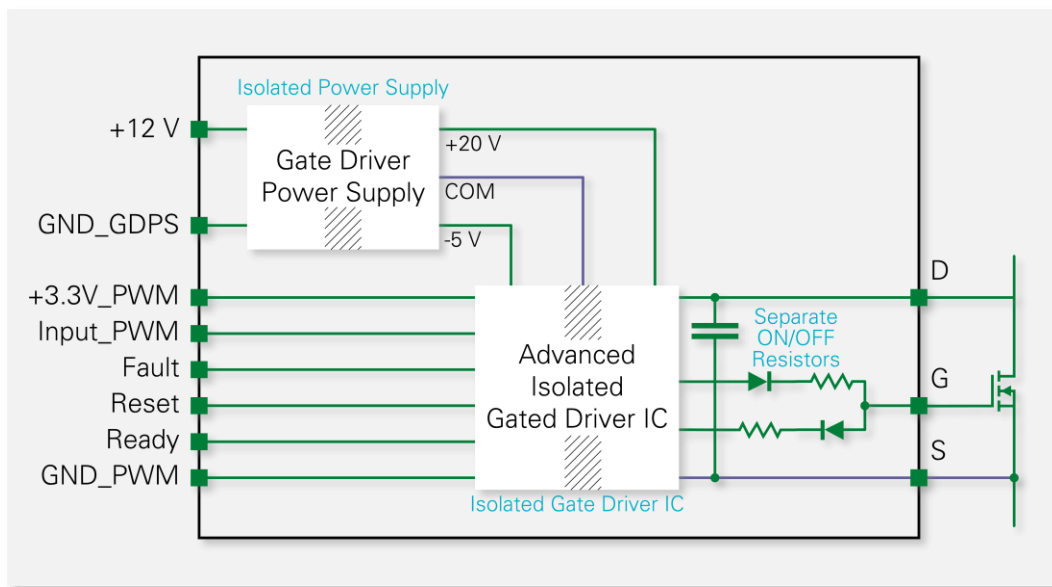
5.2. Integrated Gate Driver Modules with Protection Functions

In addition to basic driving functions, the gate driving circuitry can have protection functions to guard against fault conditions. In real applications, these functions are commonly implemented at the IC level. There are many integrated gate driver ICs with common protection features that include de-saturation (de-sat) protection, soft turn-off during FAULT, Miller clamping, and undervoltage lock out (UVLO). Many off-the-shelf driver ICs, which are typically designed for IGBT applications, can also be used for SiC MOSFETs; however, some additional considerations must be observed to guarantee the driver IC performance sufficiently matches the performance of the SiC devices.

Littelfuse provides a number of gate driver reference designs to demonstrate the performance of the off-the-shelf ICs with Littelfuse SiC MOSFETs. A custom PCB is designed for various integrated gate driver ICs from different IC vendors. These gate driver boards have the same signal interface that can be directly connected to the GDEV motherboard. This allows for a fair comparison of the performance of the different integrated driver ICs under well-defined and optimized test conditions.

Figure 8 shows the block diagram schematic of an integrated gate driver module with protection functions. It includes an isolated DC-DC power supply that converts a 12 V DC input voltage to +20 V and -5 V for the driving circuit. For performance comparison purposes, different isolated gate driver ICs with advanced functions are implemented under the same design considerations. Separate ON/OFF resistors allow controlling device turn-on and turn-off speed independently. In addition to the 12 V DC input voltage required by the isolated power supply, the driver board requires a +3.3 V DC input voltage to power the primary side of the isolated gate driver IC. The PWM input (Input_PWM/GND_PWM) requires a +3.3 V digital input. Depending on the driver IC, the input signals might also include a fault signal, reset signal, and/or ready signal.

Figure 8. Circuit Schematic of Integrated Driver with Protection Functions



The gate driver modules have three outputs, 'D', 'G', and 'S', that represent the Drain, Gate, and Source of the SiC MOSFET respectively. A probe-tip adapter is designed into the PCB in order to collect an accurate gate-source voltage measurement. The input and output connectors are 2x7 position header connectors whose mechanical dimensions and pinouts match the GDEV mother board connectors. An example gate driver module is shown in Figure 9.

Figure 9. LSICRD-GD-ISO5852 Gate Driver Modules



(a) Top side view



(b) Bottom side view

5.2.1. Key Components and IC Selection

Gate Driver Power Supply

The gate driver isolated power supply provides correct driving voltages during turn-on and turn-off states. It should also provide good isolation for noise propagation. To simplify the design and ensure good system performance, a 5.2 kV DC isolated 2 W DC-DC converter [Part Number: MGJ2D122005SC] from Murata is used in each of the Littelfuse gate drive module designs. This DC-DC converter accepts a 12 V input voltage and produces +20/-5 V dual output voltages. The isolation capacitance from input side to output side is only 3.3 pF, which provides a good isolation barrier for gate driving circuits.

Integrated Isolated Gate Driver IC with Protection Functions

Using the same design criteria, several gate driver module PCBs are designed that implement various isolated gate driver ICs with integrated protection functions. Here are the performance criteria for selecting the integrated gate driver ICs.

- **Isolation technique** – Many integrated driver ICs feature a built-in isolation barrier in the IC design. The two primary isolation technologies are optocouplers and digital isolators. Digital isolators can be further divided by way of capacitive isolation and inductive isolation. The tradeoffs between digital isolators and optocouplers have been discussed in detail previously in this application note.
- **Driving voltage** – For SiC devices, the driving voltage requirements typically tend to be higher than those associated with IGBTs. Higher driving voltages help to achieve lower conduction losses in SiC devices. It is recommended to drive the Littelfuse SiC MOSFETs with a +20 V driving voltage. Additionally, Littelfuse recommends using a -5 V signal for the off state of the Littelfuse SiC MOSFETs. A 0 V off-state driving voltage (or any voltage between -5 V and 0 V) may be used, but the power loop layout must be carefully optimized to avoid shoot-through failures.
- **Driving current** – Higher pulse current is preferred to reduce switching loss during each switching transient. Higher continuous current rating is preferred to reduce driver IC temperature during high switching frequency applications, especially with smaller external gate resistances.
- **De-sat protection** – Fast response time is required to avoid device failure and aging during shoot-through failure. De-sat protection time of less than 3 μ s – including blanking time, detection, and protection response time – can be achieved with proper gate drive design. This provides adequate protection from short circuit faults.
- **Soft turn-off during FAULT** – Slow turn-off speed is preferred in order to avoid voltage overshoot when the protection circuit turns the device off during a shoot-through failure event.
- **Active Miller clamp** – Active Miller clamping mitigates the effects of shoot-through – due to fast switching speeds of SiC MOSFETs, which causes induced gate current through the drain-gate capacitance (C_{GD}) – in a half-bridge configuration.

5.2.2. Gate Driving Layout Design

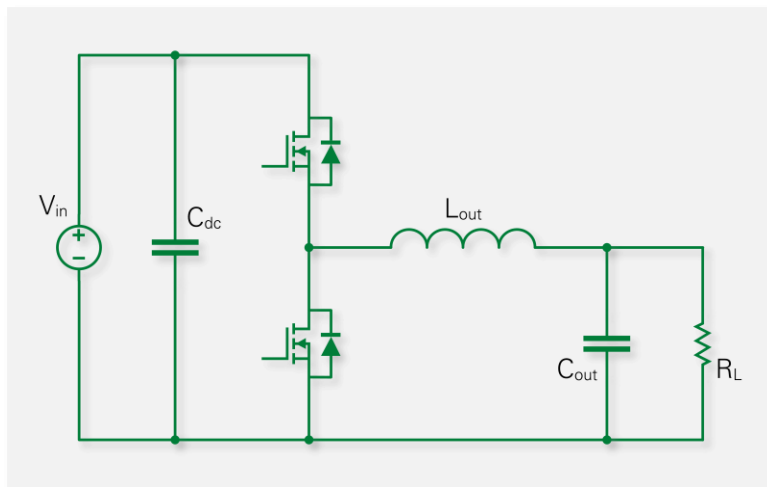
The PCB layout and routing guidelines are the same as the high current gate driver circuitry. Refer to the section titled “Gate Driving Loop Layout Design”.

6. Example Application and Test Results

6.1. Evaluation of Gate Driver Circuit Performance Under Continuous Switching

To demonstrate the performance of the gate driver circuits under continuous switching conditions, a synchronous phase-leg buck converter configuration is used as a test case. The circuit diagram is shown in Figure 10.

Figure 10. Buck Converter Block Diagram Schematic



The GDEV motherboard has four 2x7 position header connectors to provide easy connection and mechanical support for the gate driver modules. Both the high current gate driver modules and the integrated gate driver modules can easily be mounted to the 2x7 position header to drive the power MOSFETs. A 12 V DC input is needed to power the gate driver power supplies. A 24 V DC source is needed to power the on-board fan in the cooling system. The PWM signals can be provided to the gate driving modules via the header pins and a digital controller or via the SMA connectors on the gate driver board. If the integrated version gate driver is used, a 3.3 V DC input is also needed to provide power to the primary side of the driver IC. Figure 11 shows the GDEV connections for continuous switching tests.

Figure 11. GDEV Connections for Continuous Switching Tests

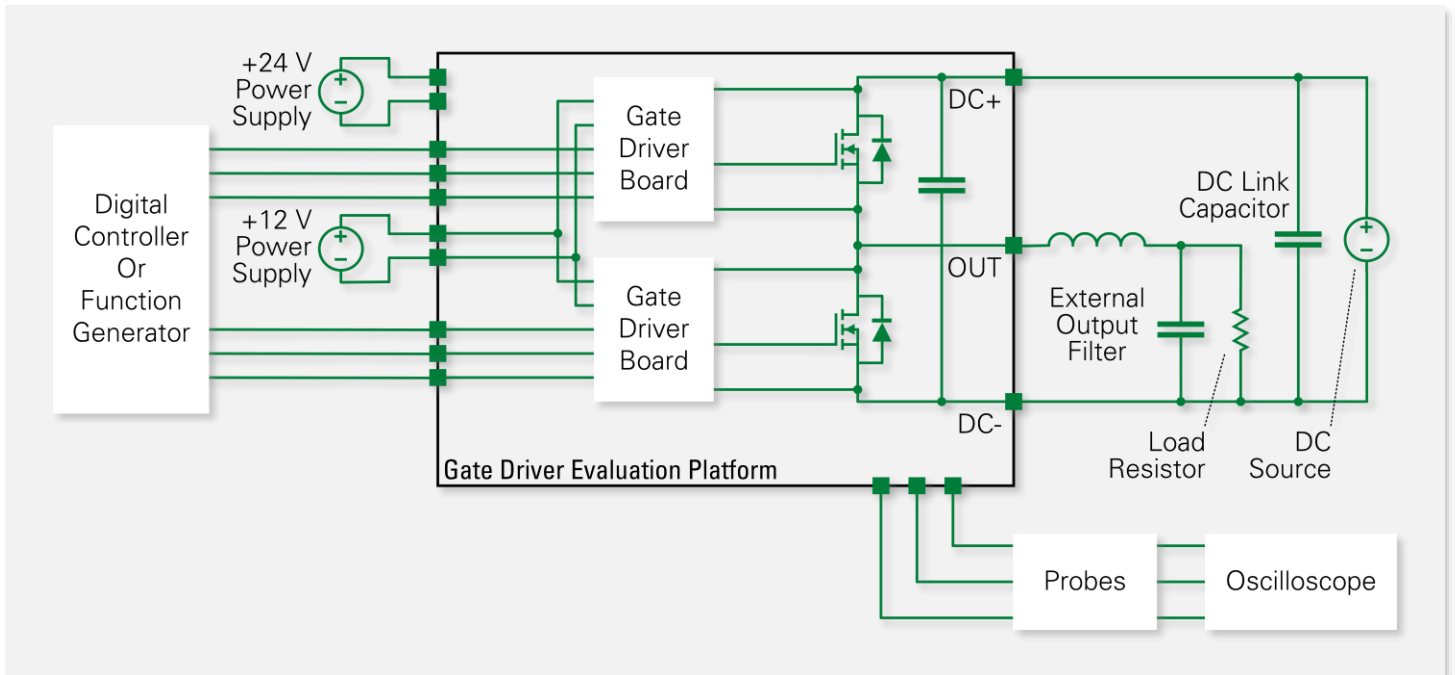
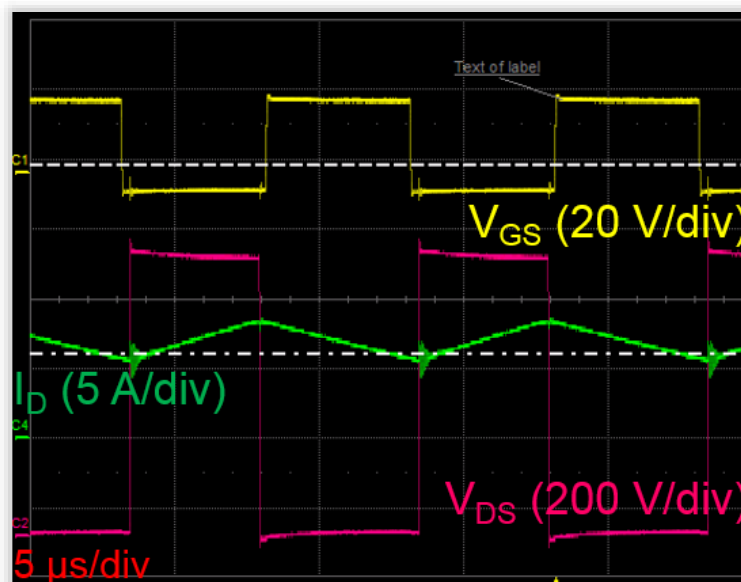


Figure 12 shows the critical waveforms during the continuous operation test with the LSICRD-GD-ISO5852 gate driver module (ISO5852S driver IC) and a 2 Ohm external gate resistance. The test conditions are: Input voltage = 800 V, Output voltage = 400 V, Switching frequency = 100 kHz, and Output power = 2.5 kW.

Figure 12. Continuous Operation Waveforms

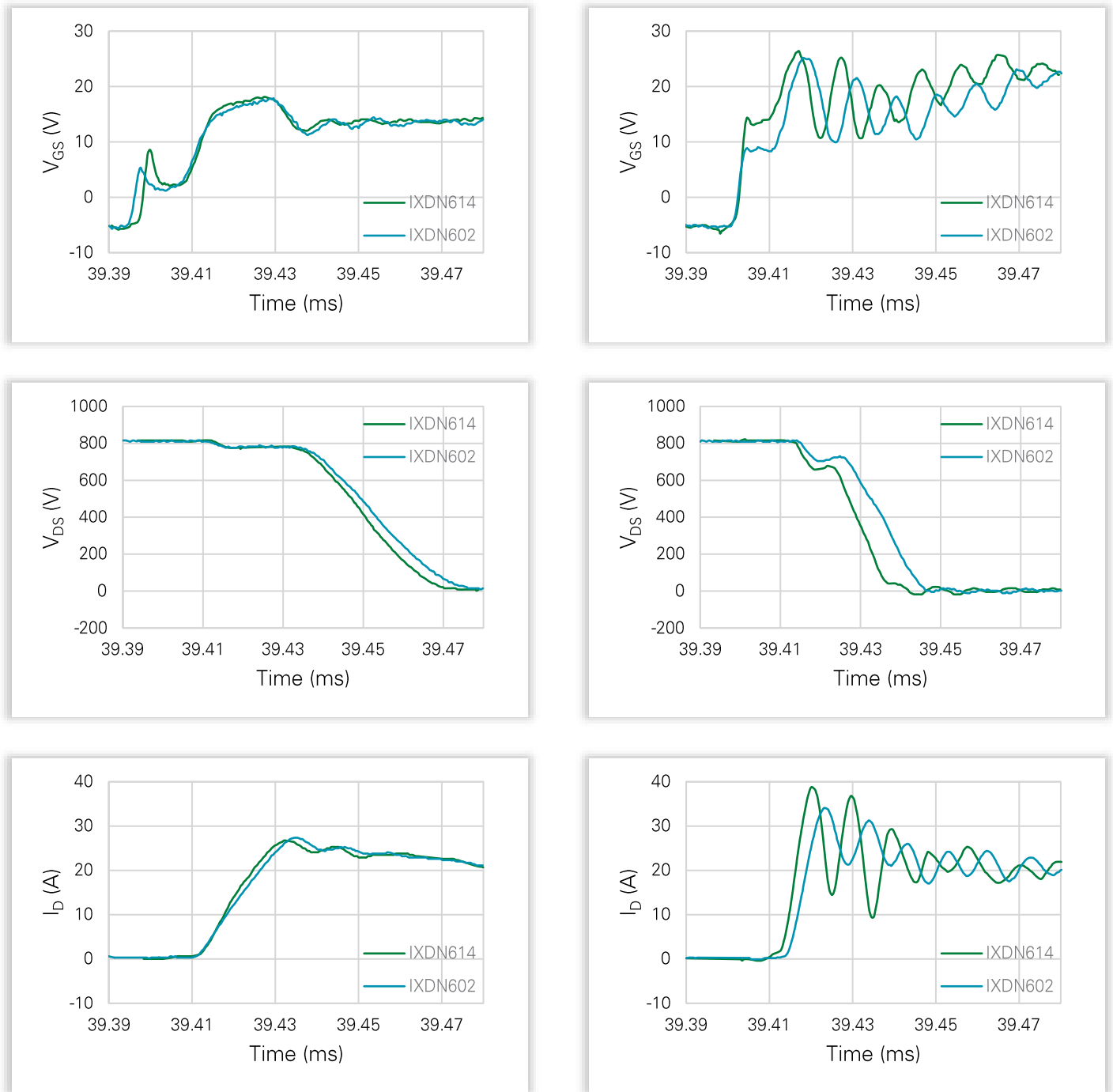


In synchronous buck converters, the low-side body diode conducts current during deadtime before the low-side MOSFET is turned on. The low-side MOSFET operates in Zero Voltage Switching (ZVS) mode and the high-side MOSFET operates in hard-switching mode. High dv/dt during fast transient events of the high-side MOSFET can affect the gate voltage on the low side MOSFET. Induced current through Miller capacitance is transferred via the gate loop, which can lead to spurious gate voltage in this topology.

6.2. Switching Loss Comparison for Driver ICs with Different Driving Capabilities

Driving capabilities of driver ICs and the external gate resistances used will influence the switching transients and the overall switching losses of SiC power MOSFETs. To measure switching loss during each switching action, the user must accurately capture the device voltage and current transients. The most precise current measurement technique uses a current viewing shunt resistor (CVR). [3] If a CVR cannot be designed into the test circuit, another current monitoring method, such as a Rogowski coil, can be used. Figure 13 shows a comparison of switching transients as a function of the IXDN614 (14 A rating) driver and IXDN602 (2 A rating) driver; the Littelfuse 1200 V, 80 mOhm SiC MOSFET was the DUT and was driven by each of the driver ICs with a 10 Ohm (Figure 13a) and a 1 Ohm (Figure 13b) gate resistor. As the figures indicate, with a small gate resistance, the switching speed of the power MOSFET is much faster if a higher current rating driver IC is used. When the external gate resistance is larger, the switching speed difference with different driver ICs is less noticeable.

Figure 13. Comparison of Switching Transients (Turn-on) between IXDN614 and IXDN602

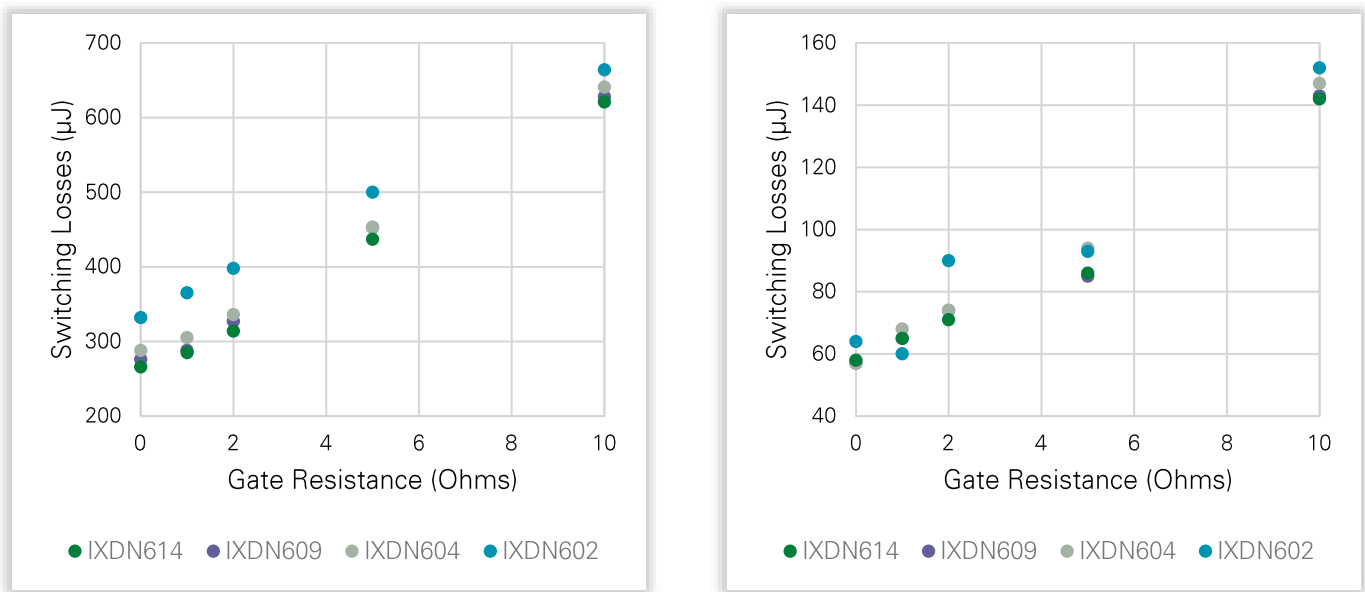


(a) 10 Ohm gate resistor

(b) 1 Ohm gate resistor

Figure 14 shows the switching loss comparison for different gate driver ICs across a range of external gate resistance values. The test conditions were $V_{DS} = 800\text{ V}$, $I_D = 20\text{ A}$. This figure also verifies that when larger external gate resistances are used, the driver IC current rate does not influence device switching loss significantly; however, when a smaller or no external gate resistance is added, the switching losses can be up to 50 percent greater if the driver IC current rating is 2 A, compared to the switching losses when a 14 A rated driver IC is used.

Figure 14. Comparison of Switching Losses Considering Gate Driver ICs and Gate Resistance



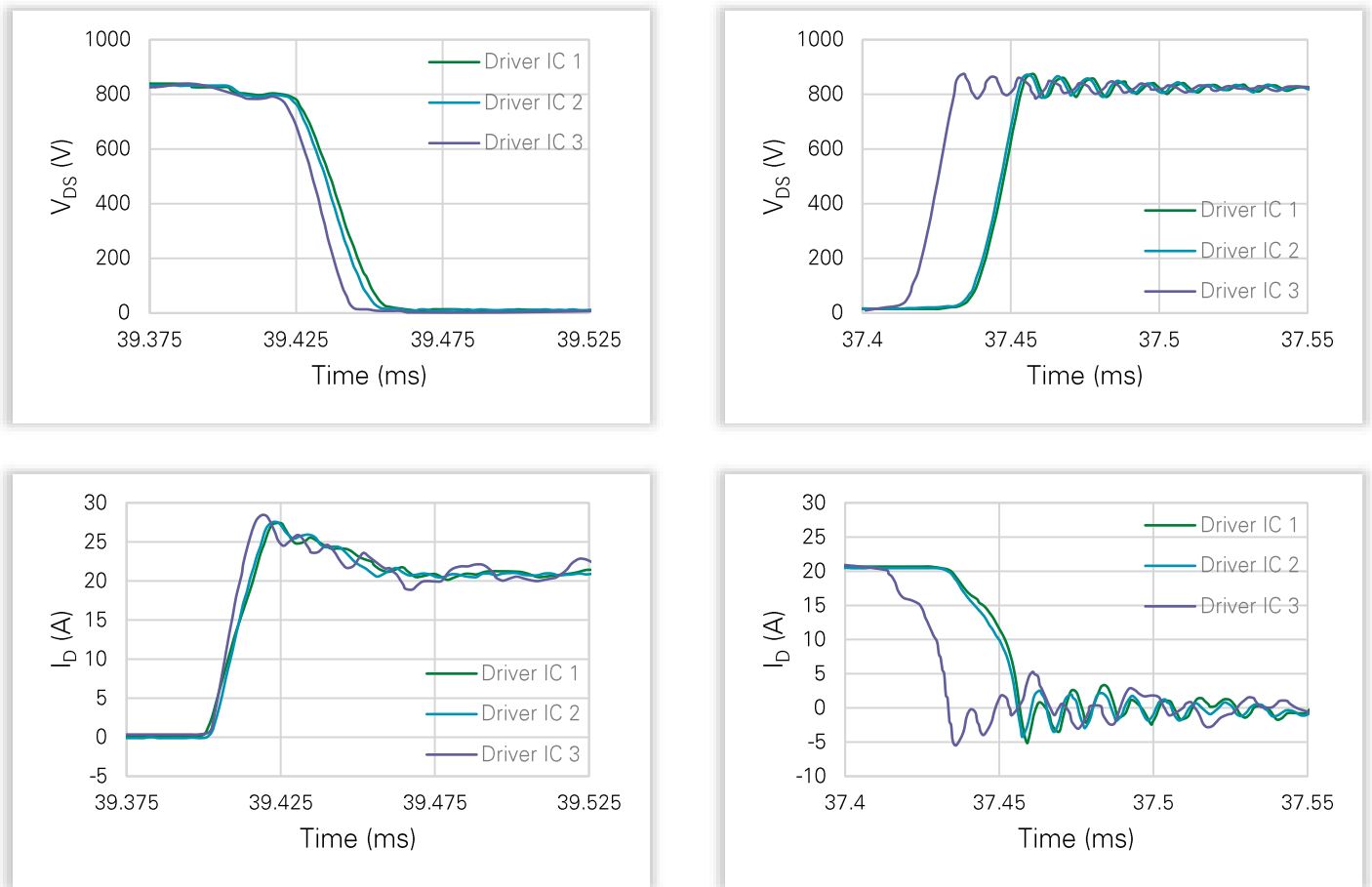
(a) Turn-on Losses

(b) Turn-off Losses

The driving current capabilities for ICs with integrated protection features are typically lower than the current capabilities of the other high current driver ICs discussed in this application note. The reported driving capability for these devices is most commonly limited by the thermal performance of the IC and is valid only under a specific set of conditions; these conditions are not typical for real application circuits.

Figure 15 and Figure 16 show a comparison of switching waveforms and turn-on losses as a function of different integrated driver ICs with a 4 A current rating under the same driving conditions (same gate resistance, same V_{DS} , and same I_D). Even though the drivers all have the same driving current rating, the switching losses are quite different. Furthermore, the difference will be even more pronounced as the gate resistance is decreased. Because of these issues, and in order to make a fair evaluation and comparison, it is recommended to test the driver IC with a power device to find the optimal pairing.

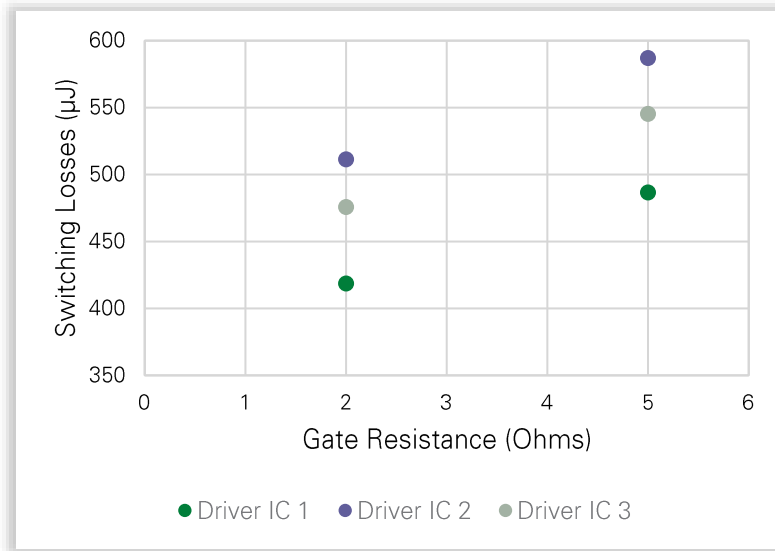
Figure 15. Waveform Comparison of Switching Transients as a Function of Driver ICs with a 4 A Current Rating Using a 2 Ohm Gate Resistor



(a) Turn-on Transient

(b) Turn-off Transient

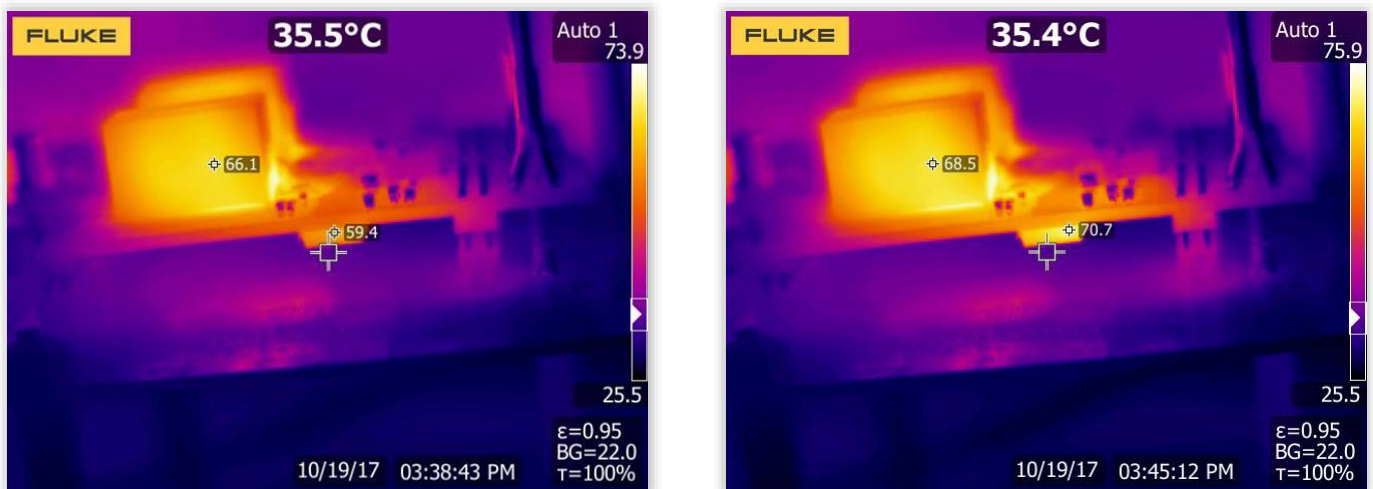
Figure 16. Turn-on Switching Loss Comparison of Driver ICs with a 4 A Current Rating



6.3. Thermal Performance of Driver ICs Under Continuous Switching

Each of the gate drive module reference designs offered by Littelfuse can be evaluated with the GDEV. The maximum switching frequency associated with a power stage design is primarily determined by the thermal performance of the phase leg and the thermal performance of the gate driver IC. Figure 17 shows the thermal image of the LSICRD-GDISO5852 with ISO5852S and 2 Ohm gate resistance operating at switching frequencies of 100 kHz (Figure 17a) and 200 kHz (Figure 17b).

Figure 17. Thermal Image of the LSICRD-GD-ISO5852 with ISO5852S and 2 Ohm Gate Resistance



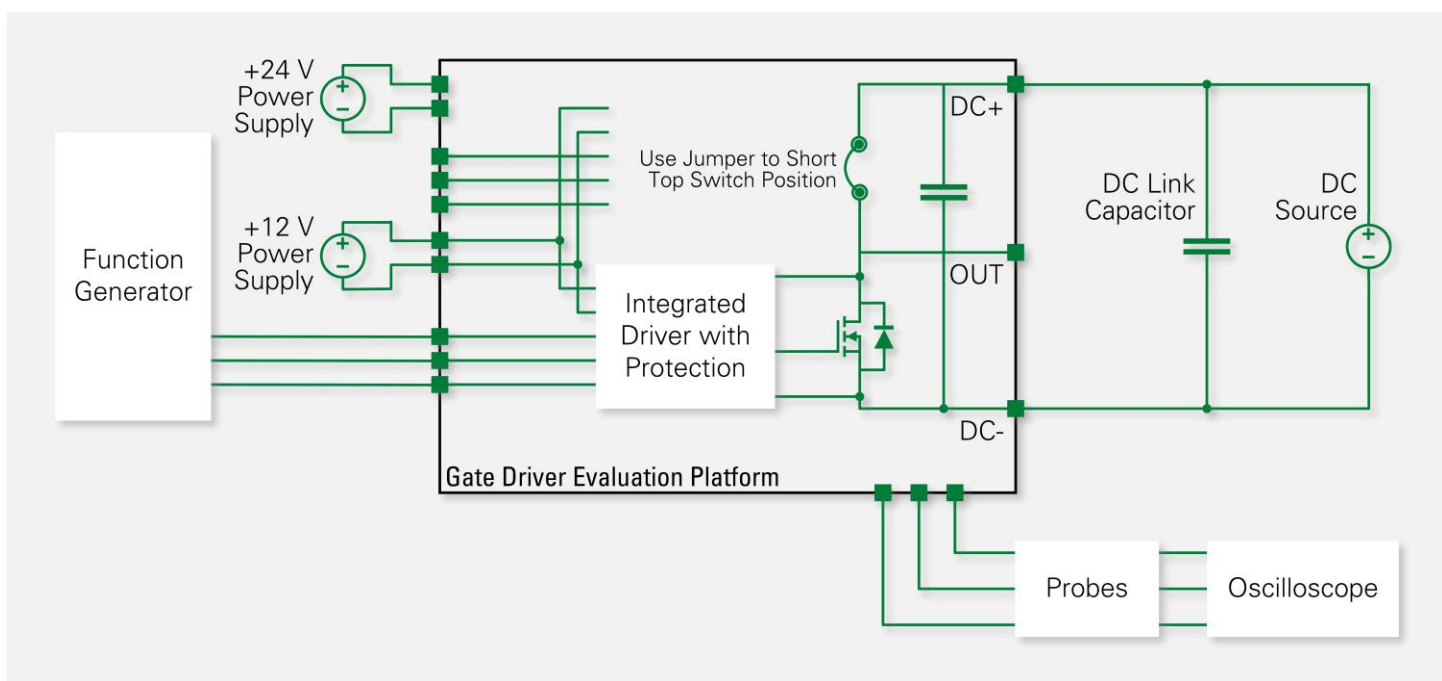
(a) $f_{sw} = 100 \text{ kHz}$

(b) $f_{sw} = 200 \text{ kHz}$

6.4. Evaluation of De-sat Protection Functions

The GDEV can also be used to evaluate de-sat protection functions of integrated gate driver ICs. Figure 18 shows the system connection for a single device short-circuit test. A function generator is used to trigger the device under test (DUT) to on. With the top switch position shorted, the gate driver circuitry of the bottom switch is relied upon to recognize the short-circuit event and turn the device off safely. The probe-tip adapter on the GDEV motherboard can be used to measure DUT drain-source voltage. The probe-tip adapter on the gate drive module can be used to measure the gate-source voltage. A Rogowski coil can be used to monitor DUT current.

Figure 18. System Connection for Single Device Short Circuit Test



The voltage drop across a MOSFET’s drain-source terminals is a linear function of the current flowing through the semiconductor. This linear relationship is characterized by the on-resistance ($R_{DS(ON)}$) of the MOSFET. Therefore, when an overcurrent event occurs, the device drain-source voltage will also increase significantly. The integrated driver IC’s de-sat protection function can sense the MOSFET drain-source voltage. If the protection threshold voltage is set properly, the IC will detect an overcurrent event, trigger the protection function, and safely turn off the SiC MOSFET. However, there are some differences between MOSFETs and IGBTs. A MOSFET’s I-V curve, in the device on-state, exhibits the behavior of a resistor. The drain-source voltage is linearly proportional to the device current and exhibits different saturation characteristics than are commonly seen in IGBT devices. Applications with high current ripples or wide operation ranges might generate significant drain-source voltage changes that could false trigger the protection mechanism. Furthermore, the on-resistance of SiC MOSFETs varies significantly with junction temperatures, which adds to the difficulty of implementing de-sat protection with SiC MOSFETs. With most off-the shelf driver ICs, the protection threshold is typically built into the IC and the real threshold is controlled by the on-state voltage drop of the blocking diodes.

For SiC MOSFETs, the fault triggering threshold voltage must be selected carefully to avoid false triggering but also to protect devices effectively under actual overcurrent conditions. IGBTs typically exhibit good short-circuit withstanding

performance due to their saturation features and larger relative die sizes. IGBTs can typically withstand more than 10 μs during a shoot-through failure. Therefore, the system only requires the driver IC to detect the event and turn off the IGBT within 10 μs . SiC MOSFETs have much shorter withstanding times. A single pulse withstanding time is typically shorter than 5 μs . This requires the driver IC to have much faster detection and response time. Considering the aging effects of devices subjected to repetitive short-circuit conditions, selecting a driver IC with a response time of less than 3 μs is recommended to ensure the effective protection of the SiC MOSFETs.

It should be noted that due to the parasitic inductance in the power loop, which resonates with the junction capacitances and other parasitic capacitances in the circuit, there will be drain-source voltage ringing after each turning on action. To avoid false triggering of the overcurrent protection functions, a certain blanking time is necessary between the turning on action and the time for which overcurrent protection functions should be active. The blanking time can be controlled by an R-C circuit, as shown in Figure 19. Given that IGBT devices switch slower, the power stage layout does not need to be fully optimized and the ringing frequency after switching is also lower. Therefore, the blanking time is greater for IGBT applications (usually longer than 250 ns). SiC MOSFETs switch well within 20 ns and require a good power loop layout design. This means the voltage ringing after switching settles much faster; thus, there is no need for a long blanking time. Selecting blanking circuit parameters carefully to match with the switching performance of the SiC MOSFETs is recommended.

Figure 19. Typical Application Circuit for Driver ICs with De-sat Protection

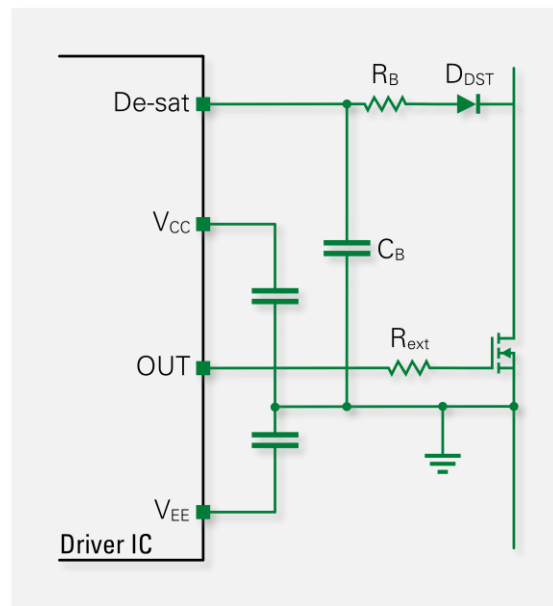
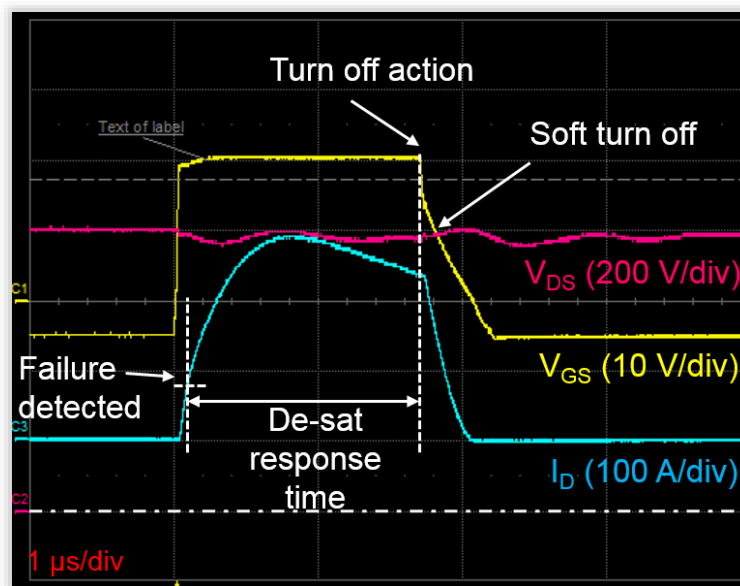


Figure 20 shows the test results of a single device short-circuit with de-sat protection. The results indicate that the off-the-shelf integrated driver IC can effectively protect the SiC MOSFET during a single device short-circuit failure. Under shoot-through conditions, the SiC MOSFET still performs as a resistor and the peak current is very high. The peak current is determined by the on-resistance and the drain-source voltage across the device. When the device junction heats up (due to the I^2R power dissipation), the device on-resistance increases and the short circuit current decreases accordingly. The response time is approximately 2 μs when the blanking time is set to 100 ns.

Figure 20. Single Device Short Circuit Test with De-sat Protection



These test results also show that during a shoot-through event, the driver IC slows down the driving speed and the gate voltage drops from +20 V to -5 V much slower than in normal operation. This is the soft turn-off function. When a shoot-through fault happens, device current increases dramatically. If the device is turned off at its normal speed, the di/dt would be much higher than it is in normal operation. Although the power loop is optimized for the high di/dt signals seen during normal operation (to mitigate drain-source voltage overshoot), it is still not enough to prevent a massive drain-source voltage overshoot, which would occur due to a higher di/dt that would be generated if a driver IC were to abruptly turn off a device during a shoot-through event. That type of drain-source overshoot could lead to device overvoltage, which could potentially damage the device. To prevent that situation from occurring, many of the integrated driver ICs have a soft turn-off function that is triggered when an overcurrent event takes place. The driver IC will turn off the device much slower than in normal operation to protect the device from over voltage failure. Because SiC MOSFETs switch much faster than IGBTs, this function is highly recommended for integrated gate driver IC selection.

7. Summary

The Gate Driver Evaluation Platform (GDEV) was designed to demonstrate the continuous operation of SiC power MOSFETs and diodes in a half-bridge configuration. Additionally, it provides a well-defined testing environment to evaluate and compare the performance of various driving board designs, as well as driver ICs. A full thermal management solution – via a heatsink – allows for the continuous operation of the power devices under rated voltage and current conditions.

The GDEV system consists of a motherboard onto which gate driver module boards can be inserted quickly and easily. The modular gate driver boards and simplified interface strategy were chosen to optimize the functionality of this platform. This application note has detailed the GDEV system architecture, presented several gate driver IC options and their technology characteristics, and provided an example application of using the GDEV to evaluate the performance of SiC power MOSFETs and various gate driver ICs under continuous switching conditions.

8. References

- [1] Silicon Lab, Application Note “CMOS Digital Isolators Supersede Optocouplers in Industrial Applications”.
- [2] Texas Instruments Inc., Application Report SLLA198 “The ISO72x Family of High-Speed Digital Isolators”.
- [3] Littelfuse, Inc., Application Note, “Dynamic Characterization Platform”.

For additional information please visit www.Littelfuse.com/powersemi

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