FG50V

Reference Design

Wi-Fi/BT Module Series

Rev. FG50V_Reference_Design_V1.0

Date: 2019-11-15

Status: Preliminary

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About the Document

History

Revision	Date	Author	Description
1.0	2019-11-15	Jared WANG/ Felix FU	Initial

Contents

1 Reference Design

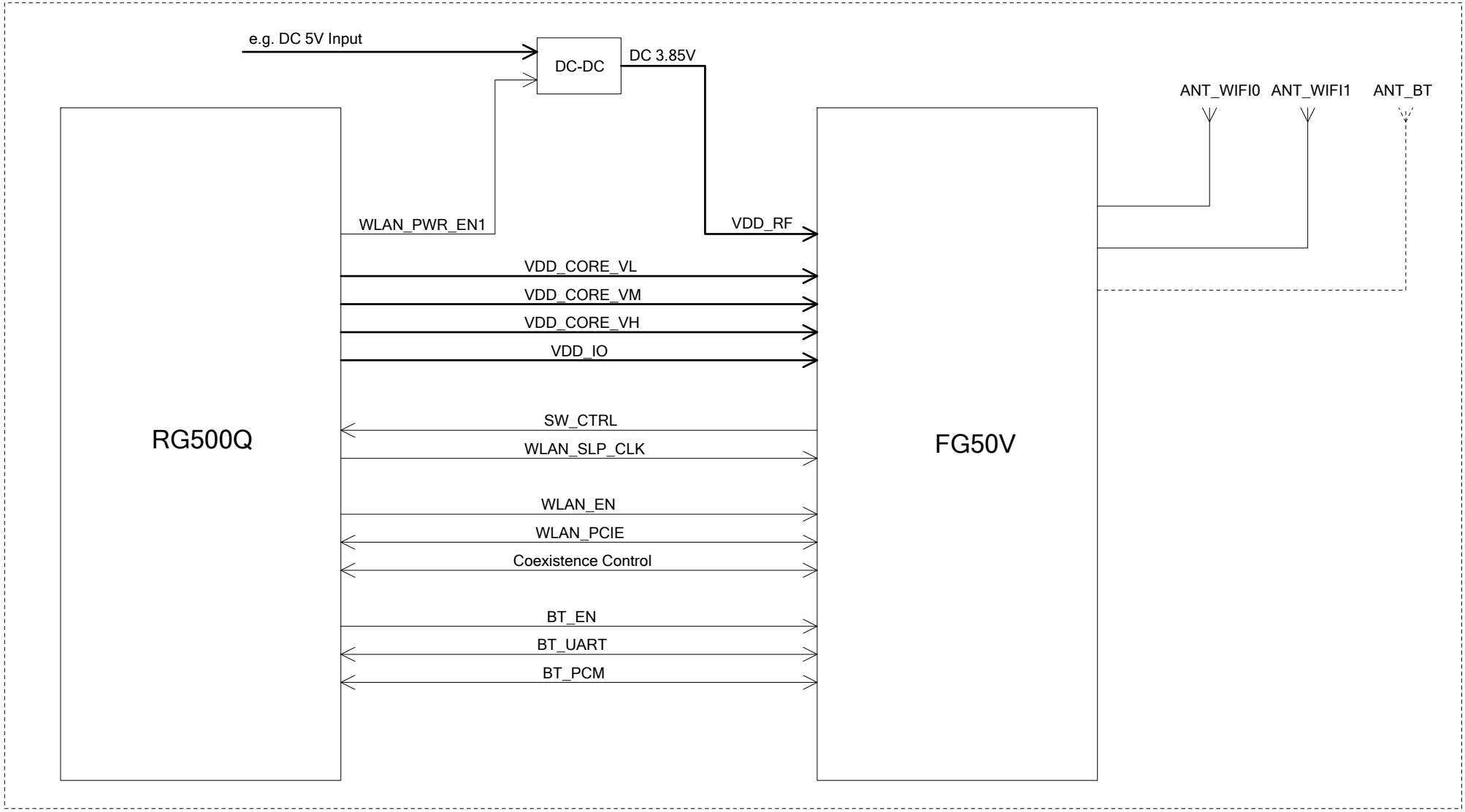
1.1. Introduction

This document provides the reference design of Quectel Wi-Fi/BT module FG50V, including the FG50V and RG500Q connection diagram, power supply designs, RF designs and other interface designs.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

FG50V and RG500Q Connection Diagram



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CHECKED BY Oscar LIU	SIZE A2	VER 1.0
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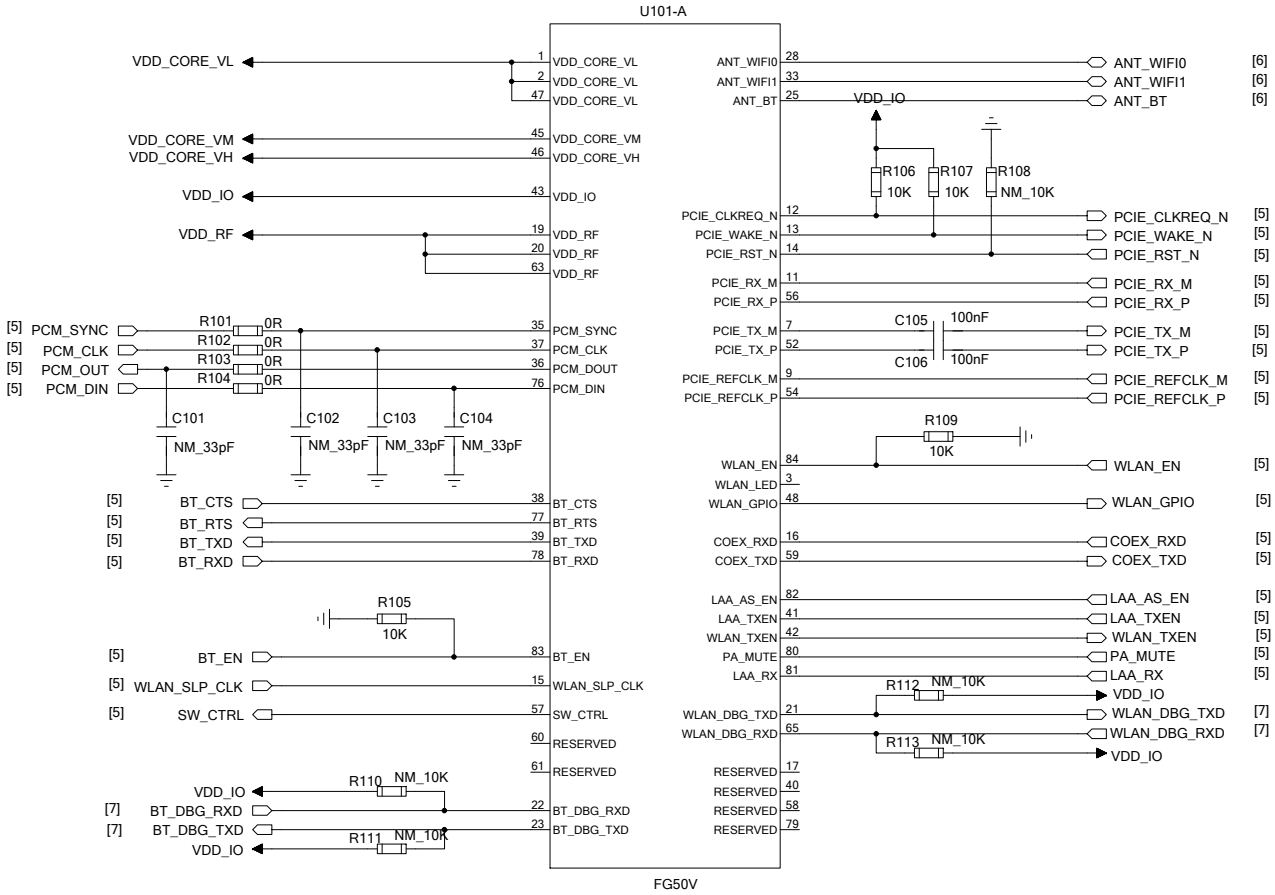
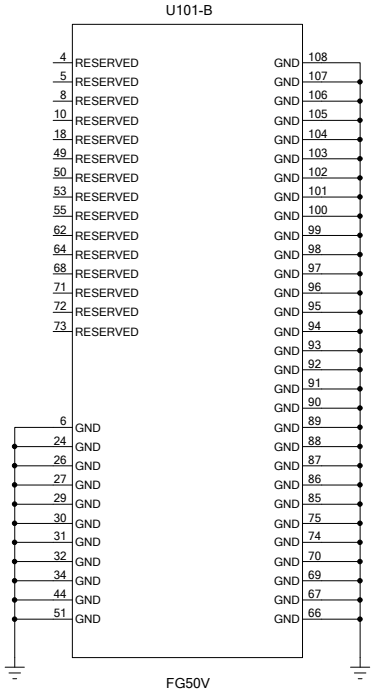
FG50V Interfaces





Notes:

1. Keep all RESERVED and unused pins unconnected.
2. The impedance of the RF signal traces must be controlled as 50Ω while routing.

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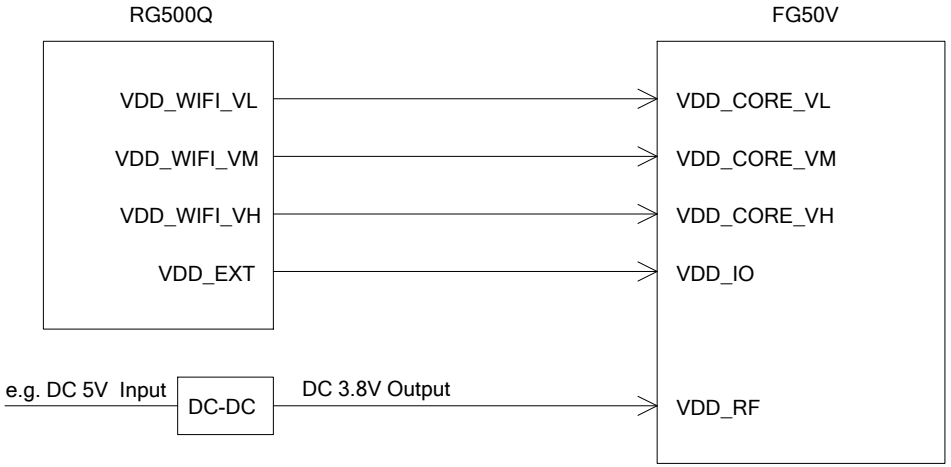
Power Design (Part 1)

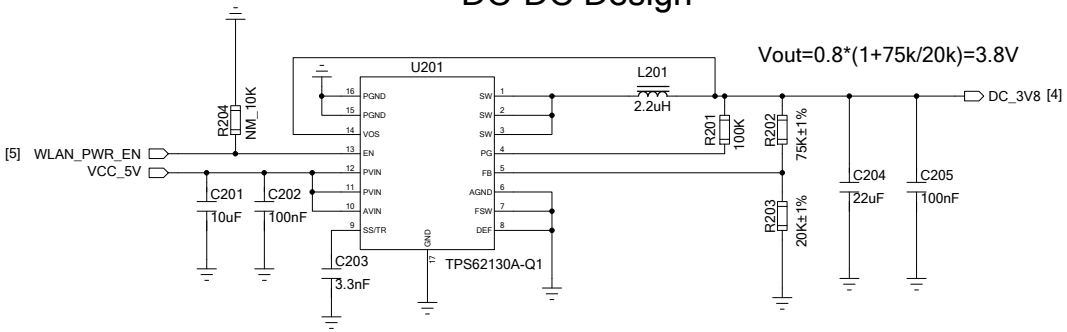
DC-DC Application



Note:

VDD_RF power supply of FG50V should be able to provide 2A current at least.

DC-DC Design



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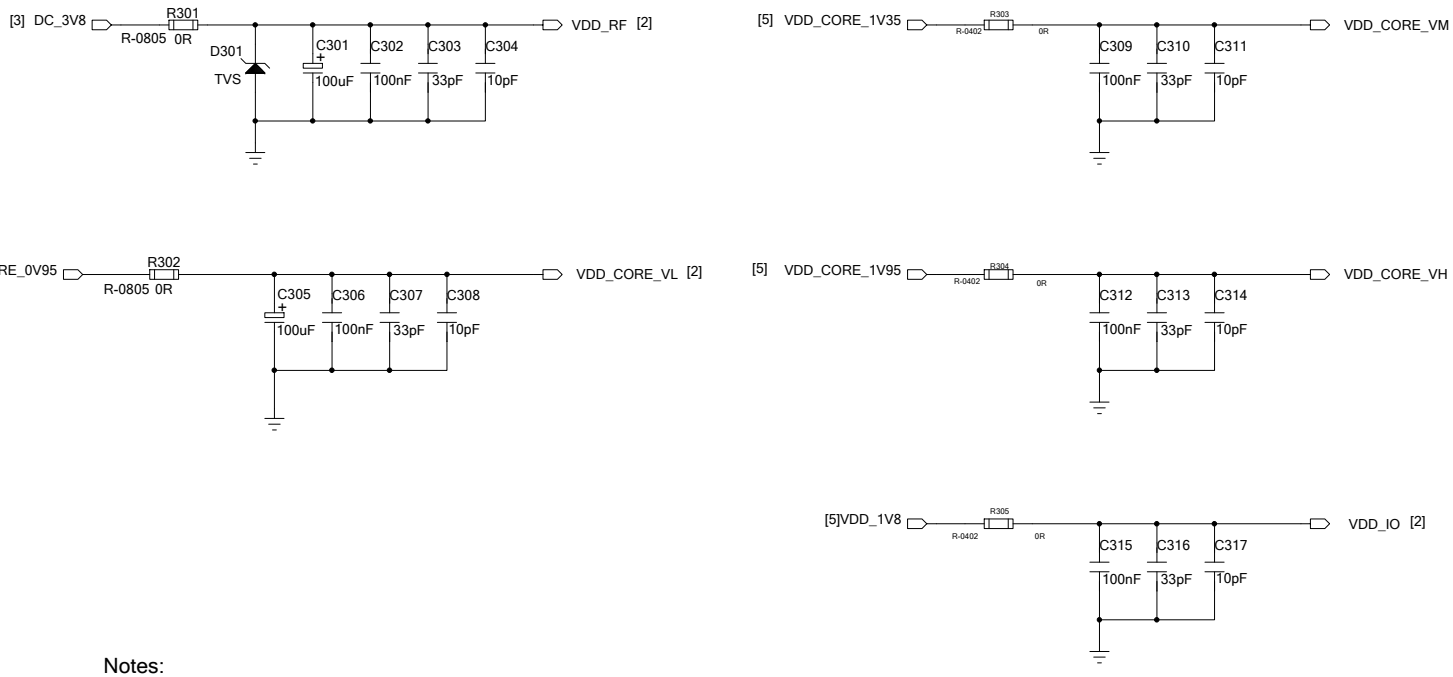
Power Design (Part 2)



Notes:

1. The recommended operating voltage of VDD_RF is 3.3V to 4.25V.
2. The TVS and decoupling capacitances should be placed close to the module's VDD pins.

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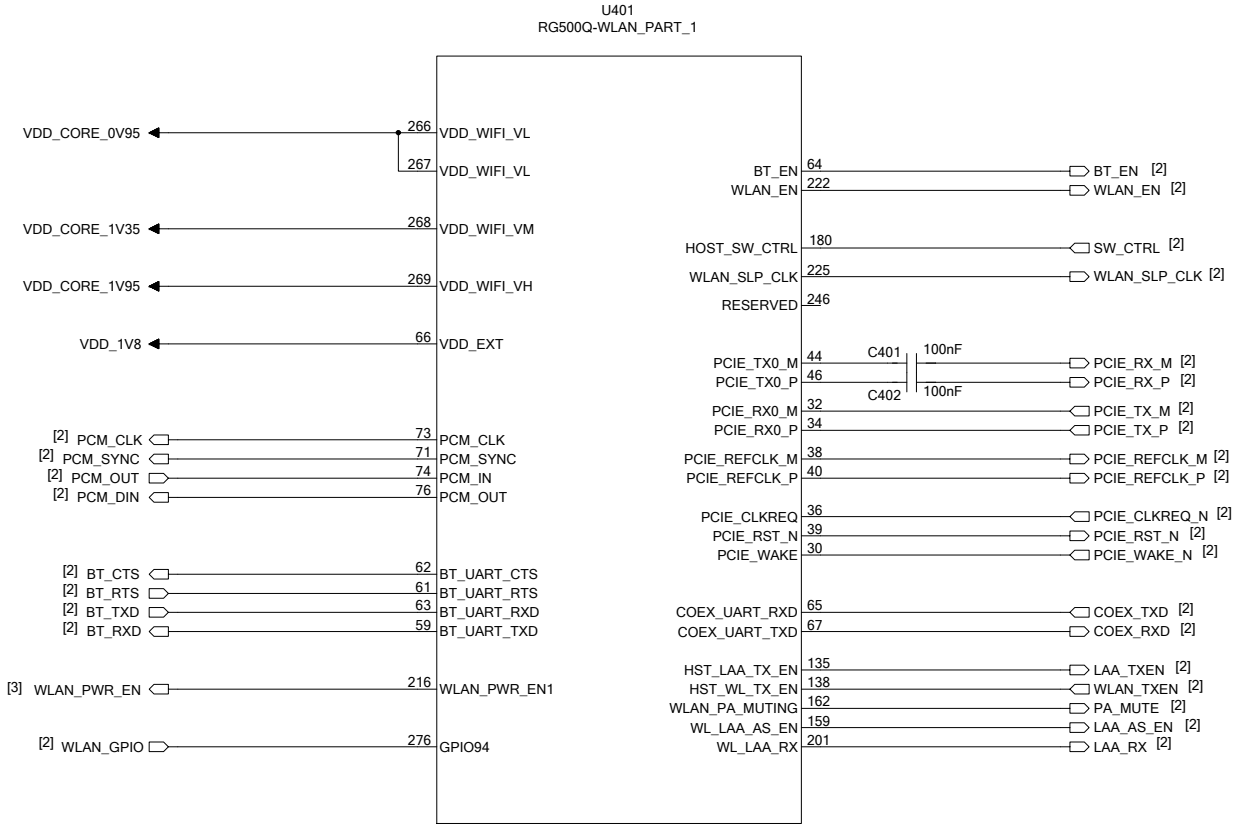
RG500Q Interfaces



Notes:

1. This is only an sketch diagram of RG500Q. For more details, please refer to *Quectel_RG500Q_Reference_Design*.
2. Keep the pin 246 (RESERVED) unconnected.

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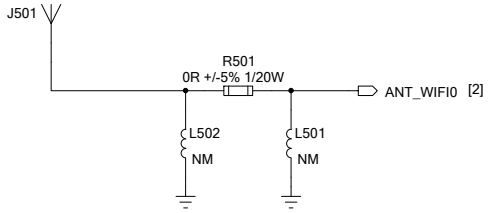
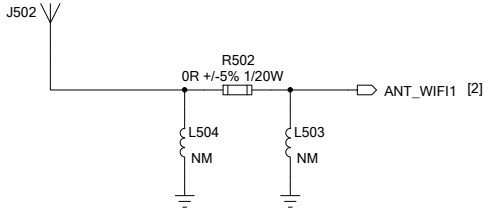
RF Antenna Designs

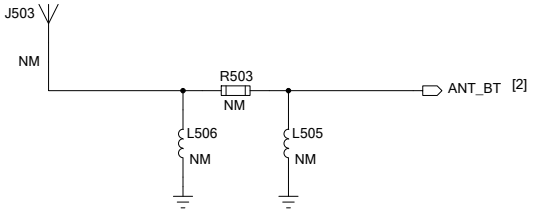
WLAN Antenna 0



WLAN Antenna 1



Dedicated BT Antenna



Notes:

1. All RF traces (microstrip on top layer and stripline for inner layer) should be cleanly routed, typically with ground cleared above and below to allow a wider 50Ω trace.
2. To facilitate future debugging, it is recommended to add a π type matching circuit during the antenna circuit design.
3. The dedicated BT antenna circuit is reserved for future debugging, and may not be used in practical applications.

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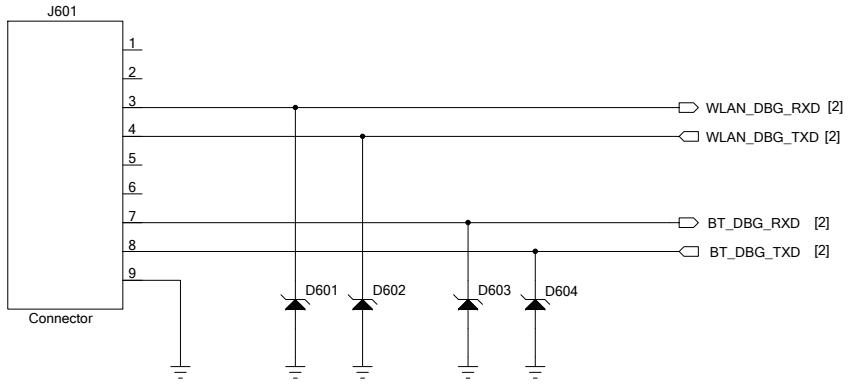
Test Points

Reserved Test Points



Notes:

1. It is recommended to reserve the test points for debug UART to facilitate future debugging.
2. The power domain of debug UART is 1.8V. A voltage-level translator should be used if the power domain of customer application is 3.3V.

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