Features

- Precision low voltage monitoring and Power Fail detector
- 200ms (typical) reset timeout
- Manual reset input
- Independent watchdog timer
- Reset output stage
- Push-pull Active-low output (TPV706)
- Low power consumption: 4 μA
- Guaranteed reset output valid to VCC = 1 V
- Power supply glitch immunity
- Specified from −40°C to +125°C
- 8-lead SOP package

Applications

- Microprocessor systems
- Computers
- Controllers
- Intelligent Instruments
- Portable equipment

Description

The TPV706 is a supervisory circuit that monitors power supply voltage levels and provides a power-on reset signal.

A watchdog monitor is provided, which is activated if the watchdog input doesn't toggle within 1.6 sec.

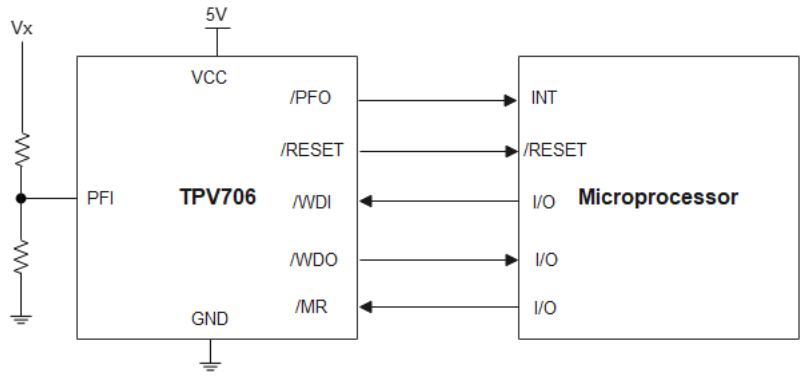
A reset signal can also be asserted by an external manual reset input.

In addition, there is a power fail detector with 1.25V threshold, which can be used to monitor an additional power supply.

The reset periods are fixed at 200 ms (typical).

The TPV706 is available in a 8-lead SOP package and typically consumes only 4 μA, suitable for use in low power, portable applications.

Typical Application Circuit



Product Family Table

Order Number	Reset Threshold Voltage (V)	Package Marking	Package
TPV706VL1-SR(1)	1.58	V6V	SOP-8
TPV706WL1-SR(1)	1.67	V6W	SOP-8
TPV706YL1-SR(1)	2.19	V6Y	SOP-8
TPV706ZL1-SR(1)	2.32	V6Z	SOP-8
TPV706RL1-SR(1)	2.63	V6R	SOP-8
TPV706SL1-SR	2.93	V6S	SOP-8
TPV706TL1-SR(1)	3.08	V6T	SOP-8
TPV706ML1-SR(1)	4.38	V6M	SOP-8
TPV706LL1-SR(1)	4.63	V6L	SOP-8

(1) Future product, contact 3PEAK factory for more information and sample.

Table of Contents

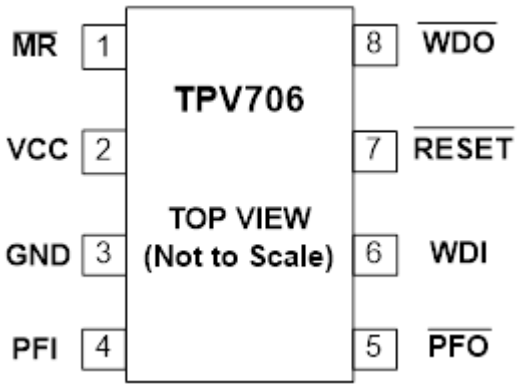
Revision History

Date	Revision	Notes
2019/1/1	Rev.A.01	Initial version.
2019/5/28	Rev.A.02	Add WDI pulse interval spec.
2022/6/25	Rev.A.3	Update note for MR input pulse width, update to latest datasheet format and add WDI to /WDO time information.

Pin Configuration and Functions

SOP-8 Package

Top View



Pin Functions

Pin		I/O	Description
No.	Name		
1	$\overline{MR}$	I	Manual Reset Input. This is an active-low input, which generates a reset when forced low for at least 1 μs. It features an internal pull-up current.
2	VCC	I	Power Supply Voltage being Monitored.
3	GND	-	Ground.
4	PFI	I	Power Fail Input. When PFI is less than 1.25 V, PFO goes low. If unused, connect PFI connects to GND.
5	$\overline{PFO}$	O	Power-Fail Output. It goes low when PFI is less than 1.25V; otherwise stays high.
6	WDI	I	Watchdog Input. Generates a reset if the voltage on the pin remains low or high for the duration of the watchdog timeout. The timer is cleared if a logic transition occurs on this pin or if a reset is generated. Floating WDI disables the watchdog function.
7	$\overline{RESET}$	O	Active-Low Reset Push-Pull Output Stage. Asserted whenever VCC is below the reset threshold or by a low signal on the $\overline{MR}$ input. It remains low for 200mS after VCC goes above the reset threshold or $\overline{MR}$ goes from low to high. A watchdog timeout does not trigger $\overline{RESET}$.
8	$\overline{WDO}$	O	Watchdog Output. Pulls low if WDI remains low or high for the duration of the watchdog timeout, and does not go high again until the watchdog is cleared. Whenever VCC is below the reset threshold, $\overline{WDO}$ stays low. As soon as VCC rises above the reset threshold, $\overline{WDO}$ goes high with no delay.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
V_{CC}		−0.3	6	V
Output Current			20	mA
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_J	Maximum Junction Temperature		150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(1) This data was taken with the JEDEC low effective thermal conductivity test board.

(2) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001(1)	4000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002(2)	2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP-8	143	60	°C/W

Electrical Characteristics

All test condition is V_{CC} = 1.53V to 5.5 V, T_A = -40°C to +125°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage and Current						
V_{CC}	Operating supply voltage		1		5.5	V
I_{CC}	Supply current	WDI and MR unconnected (VCC=1.8V)		4	15	μA
		WDI and MR unconnected (VCC=5V)		6	20	μA
V_{TH}	Reset threshold voltage	TPV706V	1.51	1.58	1.63	V
		TPV706W	1.62	1.67	1.71	V
		TPV706Y	2.12	2.19	2.25	V
		TPV706Z	2.25	2.32	2.38	V
		TPV706R	2.55	2.63	2.70	V
		TPV706S	2.82	2.93	3.00	V
		TPV706T	3.00	3.08	3.15	V
		TPV706M	4.25	4.38	4.5	V
		TPV706L	4.5	4.63	4.75	V
	Reset threshold temperature coefficient			80		ppm/°C
V_{HYS}	Reset threshold hysteresis			$2\times\frac{V_{TH}}{1000}$		mV
t_{RD}	V_{CC} to reset delay			20		μs
t_{RP}	Reset timeout period		140	200	280	ms
V_{OL}	Reset output voltage low (Push-Pull)	V_{CC} ≥ 1 V, I_{SINK} = 50 μA			0.3	V
		I_{SINK} = 1.2mA @ Vcc≥2V			0.4	V
V_{OH}	Reset output voltage high (Push-Pull)	I_{SOURCE} = 800 μA, @ V_{CC}≥5V	0.7 × V_{CC}			V
$\overline{MR}$ Pin						
V_{IL_MR}	$\overline{MR}$ input threshold V_{IL}				0.3 × V_{CC}	V
V_{IH_MR}	$\overline{MR}$ input threshold V_{IH}		0.7 × V_{CC}			V
t_{PW_MR}	$\overline{MR}$ input pulse width (1)		6			μs
t_{GR_MR}	$\overline{MR}$ glitch rejection			100		ns
t_{d_MR}	$\overline{MR}$ to reset delay			1	6	μs
I_{MR_V0}	$\overline{MR}$ pull-up current	V_{CC} = 3V		80		μA
t_{WD}	Watchdog timeout period		1	1.6	2.4	sec
t_{PW_WD}	WDI pulse width 50 ns		50			ns

Electrical Characteristics (Continued)

All test condition is V_{CC} = 1.53V to 5.5 V, T_A = -40°C to +125°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	WDI pulse interval		12			ms
V_{IL_WDI}	WDI input threshold V_{IL}				0.3 × V_{CC}	V
V_{IH_WDI}	WDI input threshold V_{IH}		0.7 × V_{CC}			V
I_{WDI}	WDI input current	V_{WDI} = V_{CC}		20		μA
		V_{WDI} = 0		-15		μA
V_{OL_WDO}	$\overline{WDO}$ V_{OL}	I_{SINK} = 1.2mA @ V_{CC}≥5V			0.4V	V
V_{OH_WDO}	$\overline{WDO}$ V_{OH}	I_{SOURCE} = 800 μA @ Vcc≥5V	0.7*V_{CC}			V
PFI and $\overline{PFO}$						
V_{TH_PFI}	Power fail input threshold	PFI falling	1.18	1.25	1.32	V
V_{OL_PFO}	$\overline{PFO}$ V_{OL}	I_{SINK} = 1.6mA @ V_{CC}≥5V			0.4V	V
V_{OH_PFO}	$\overline{PFO}$ V_{OH}	I_{SOURCE} = 800 μA @ V_{CC}≥5V	0.7*V_{CC}			V

***Note:** (1) MR pulse width given by customer in application should be longer than minimum value of MR input pulse width requirement.

Typical Performance Characteristics

All test condition: V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.

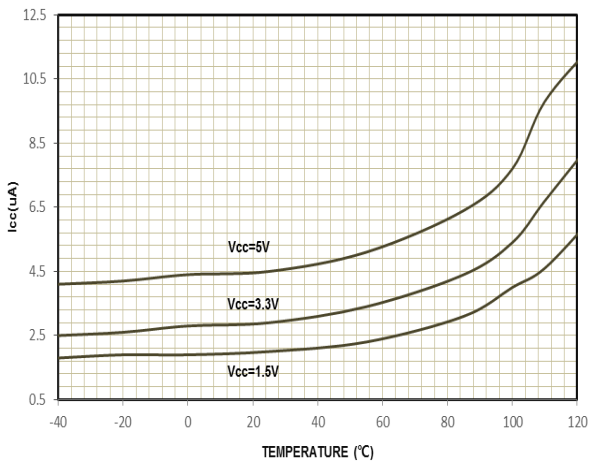


Figure 1. Supply Current vs. Temperature

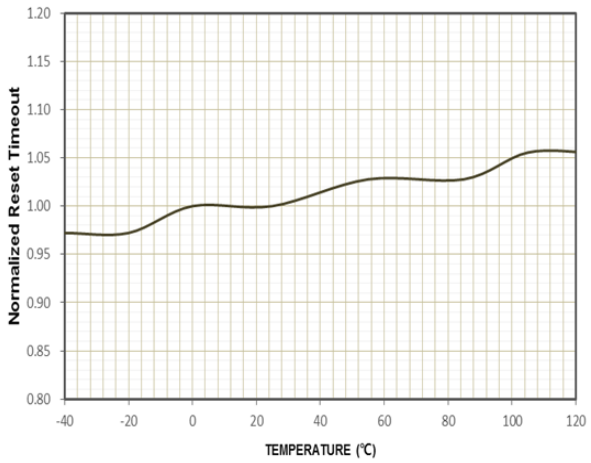


Figure 2. Normalized RESET Timeout Period vs. Temperature

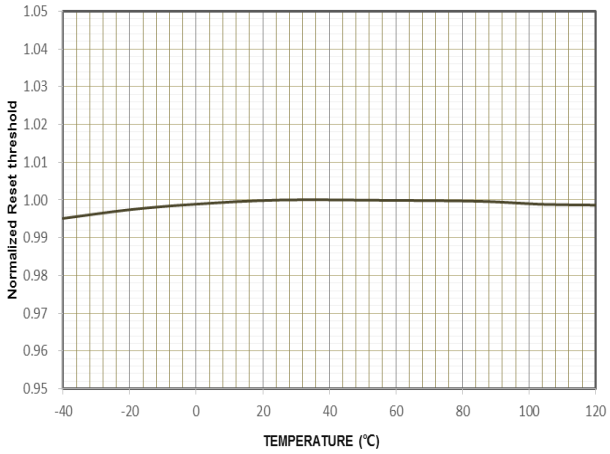


Figure 3. Normalized RESET Threshold vs. Temperature

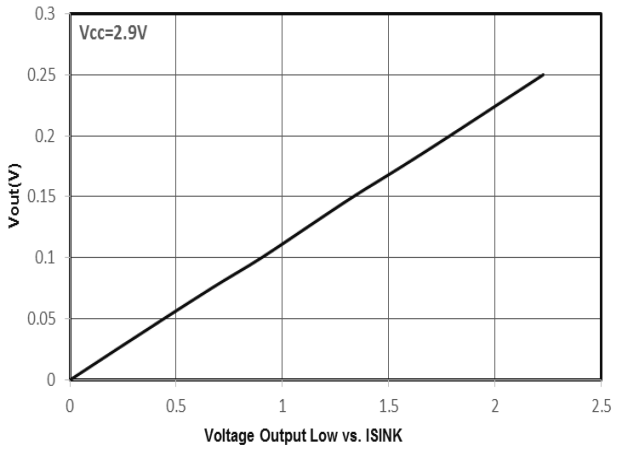


Figure 4. Voltage Output Low vs. ISINK

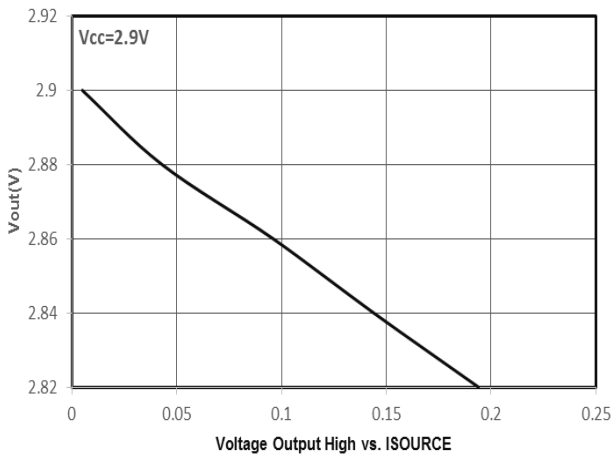


Figure 5. Voltage Output Low vs. ISOURCE

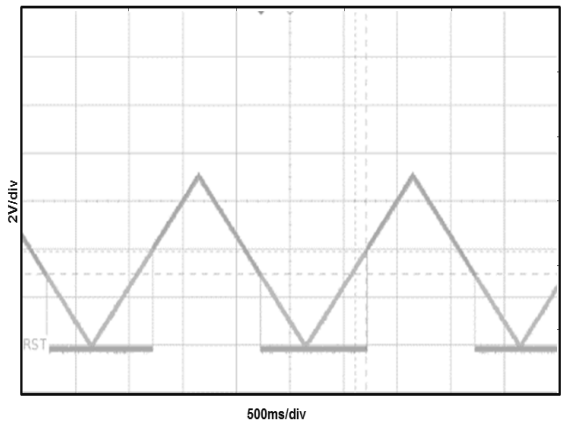


Figure 6. RESET Output Voltage vs. Supply Voltage

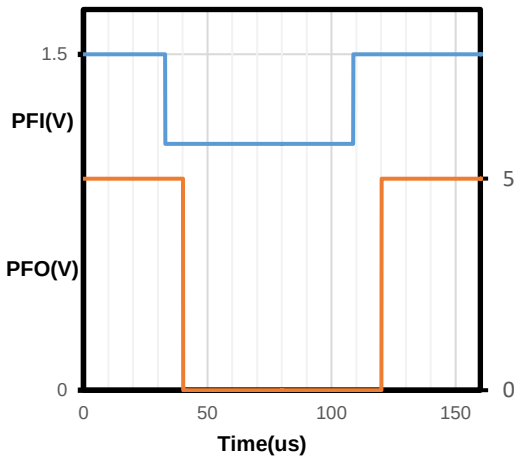


Figure 7. PFI vs. PFO

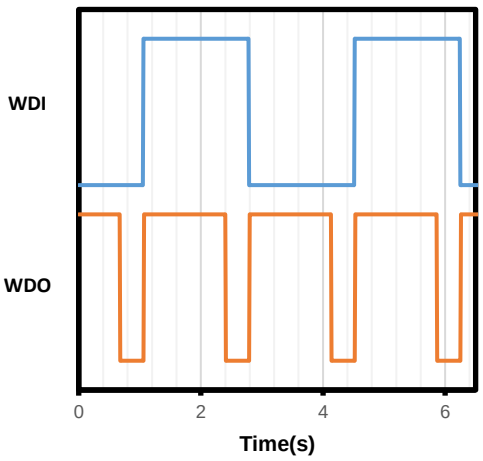


Figure 8. WDI vs. WDO

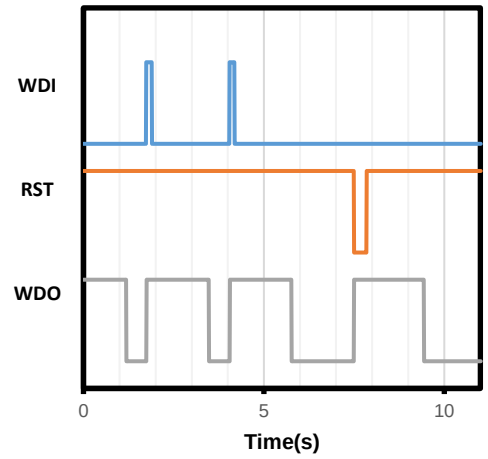


Figure 9. WDI vs. RST and WDO

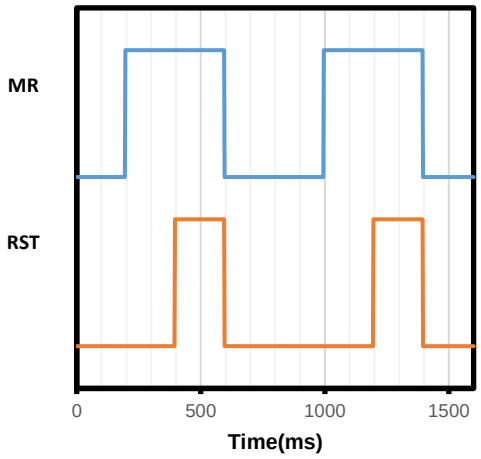


Figure 10. MR vs. RST

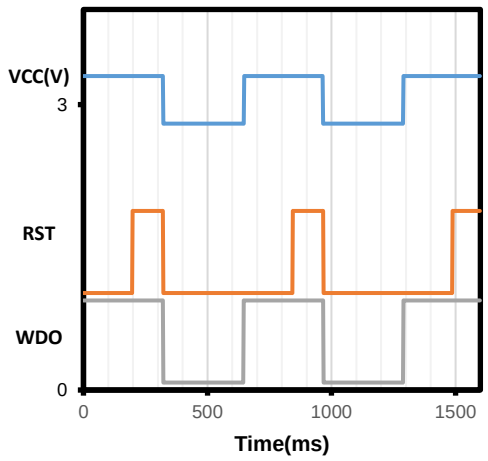


Figure 11. Vcc vs. RST and WDO

Detailed Description

Overview

The TPV706 provides supply voltage supervision, watchdog function, manual reset function as well as a 1.25V power fail comparator.

Function Block Diagram

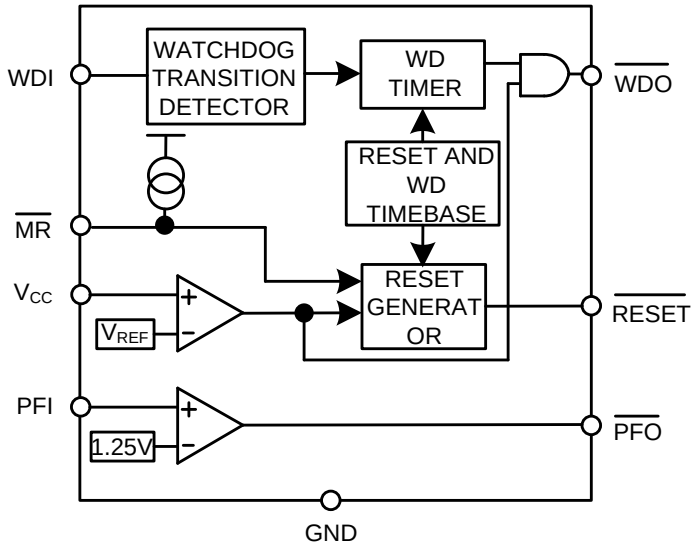


Figure 12. Block Diagram

Feature Description

RESET OUTPUT

The TPV706 features an active-low push-pull output. The reset signal is guaranteed to be logic low for V_{CC} down to 1 V. The reset output is asserted when V_{CC} is below the reset threshold (V_{TH}), or when MR is driven low. Reset remains asserted for the duration of the reset active timeout period (t_{RP}) after V_{CC} rises above the reset threshold, or after MR transitions from low to high. Figure 13 shows the reset (active low) outputs.

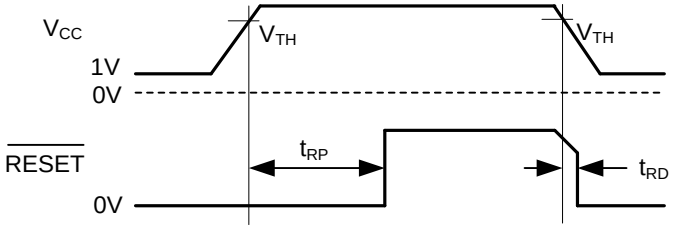


Figure 13. Reset Timing Diagram

MANUAL RESET INPUT

The TPV706 features a manual reset input (MR), which, when driven low, asserts the reset output. When MR transitions from low to high, reset remains asserted for the duration of the reset active timeout period before de-asserting.

The MR input has an internal pull-up current so that the input is always high when unconnected. Noise immunity is provided on the MR input, and fast, negative-going transients are ignored. A 0.1 µF capacitor between MR and ground provides additional noise immunity.

WATCHDOG INPUT

The TPV706 features a watchdog timer, which monitors microprocessor activity. A timer circuit is cleared with every low-to-high or high-to-low logic transition on the watchdog input pin ($\overline{WDI}$). If the timer counts through the preset watchdog timeout period (t_{WD}), the watchdog output ($\overline{WDO}$) goes low, a low to high or high to low transition on the $\overline{WDI}$ pin clears the watchdog timer. The delay time from $\overline{WDI}$ toggling to $\overline{WDO}$ going high is within 35ms. The microprocessor is required to toggle the $\overline{WDI}$ pin to avoid being reset.

Whenever VCC is below the reset threshold, $\overline{WDO}$ stays low. As soon as VCC rises above the reset threshold, $\overline{WDO}$ goes high with no delay. Figure 14 shows the watchdog timing.

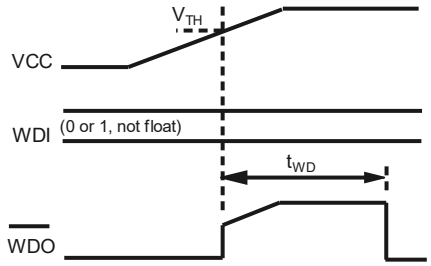


Figure 14. Watchdog Timing Diagram

POWER FAIL COMPARATOR

The power fail comparator is a 1.25V comparator, which can monitor an external power supply through a resistive divider. When the voltage on the PFI is lower than1.25 V, the comparator output goes low, indicating a power failure, which can be used as early warning of power failure.

Application and Implementation

NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

A typical application circuit is shown in following Figure.

Microprocessor activity is monitored using WDI. When the WDI remains low or high for the duration of the watchdog timeout, the WDO will trigger a manual reset from CPLD. The CPLD will drive the /MR from high to low and trigger the /RESET. When you test the duration from the /MR low to /RESET low, we promise the time is less than 12us. (Affected by the MR pulse width and MR to Reset Delay).

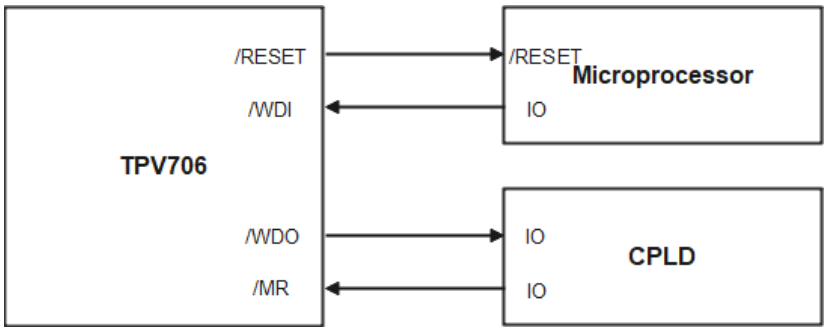
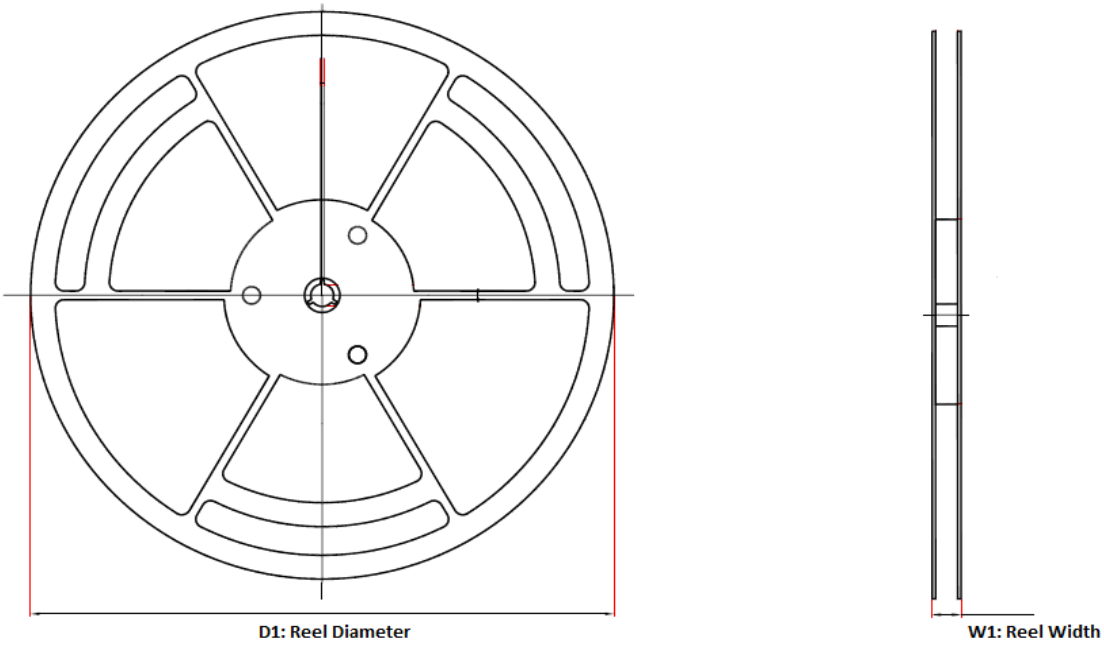


Figure 15. Typical Application Circuit

Tape and Reel Information

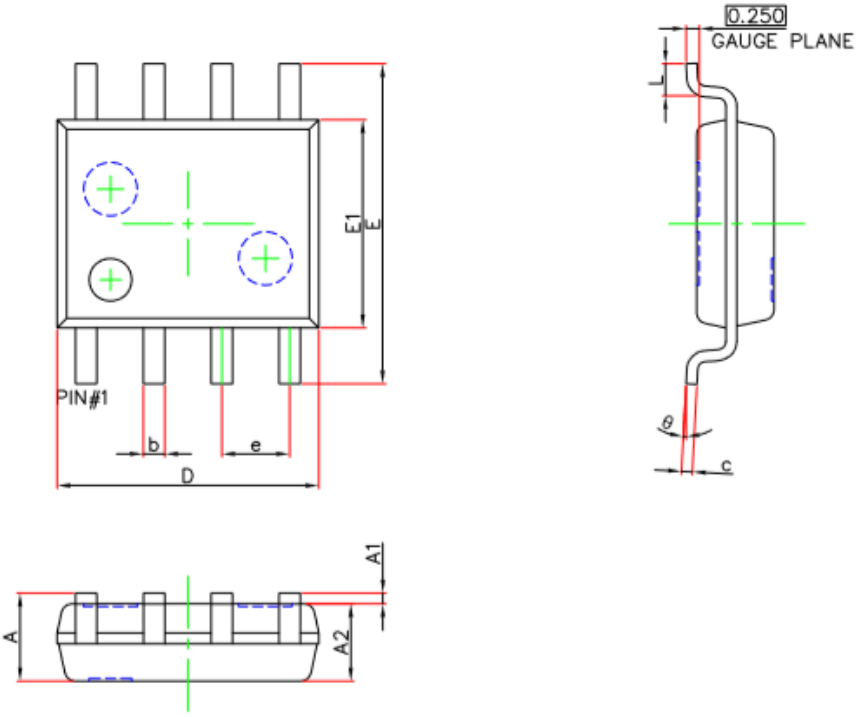


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPV706XXX-SR	SOP-8	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1

Package Outline Dimensions

SOP-8

SOP8(150mil)(12R) PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	0.800	0.016	0.031
θ	0°	8°	0°	8°

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPV706VL1-SR	−40 to 125°C	SOP-8	V6V	1	Tape and Reel, 4000	Green
TPV706WL1-SR	−40 to 125°C	SOP-8	V6W	1	Tape and Reel, 4000	Green
TPV706YL1-SR	−40 to 125°C	SOP-8	V6Y	1	Tape and Reel, 4000	Green
TPV706ZL1-SR	−40 to 125°C	SOP-8	V6Z	1	Tape and Reel, 4000	Green
TPV706RL1-SR	−40 to 125°C	SOP-8	V6R	1	Tape and Reel, 4000	Green
TPV706SL1-SR	−40 to 125°C	SOP-8	V6S	1	Tape and Reel, 4000	Green
TPV706TL1-SR	−40 to 125°C	SOP-8	V6T	1	Tape and Reel, 4000	Green
TPV706ML1-SR	−40 to 125°C	SOP-8	V6M	1	Tape and Reel, 4000	Green
TPV706LL1-SR	−40 to 125°C	SOP-8	V6L	1	Tape and Reel, 4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.