· Description

。

X130 9KHz~6GHz low-overshoot digital attenuator, which is integrated with a fixed gain attenuator, an oscillator, a charge pump, a serial-to-parallel conversion circuit, a level conversion circuit and other circuits therein, is a monolithic integrated circuit manufactured by an SOI process. No DC level is output from the RF port of the chip, and the control port thereof is compatible with TTL level. A 4mm×4mm QFN24 package is adopted.

Features

•

• Operating frequency 9KHz~6GHz

• Optional steps 0.25dB, 0.5dB and 1dB

• Max. attenuation 31.75dB

• Low insertion loss

• Low overshoot

• High linearity

Features

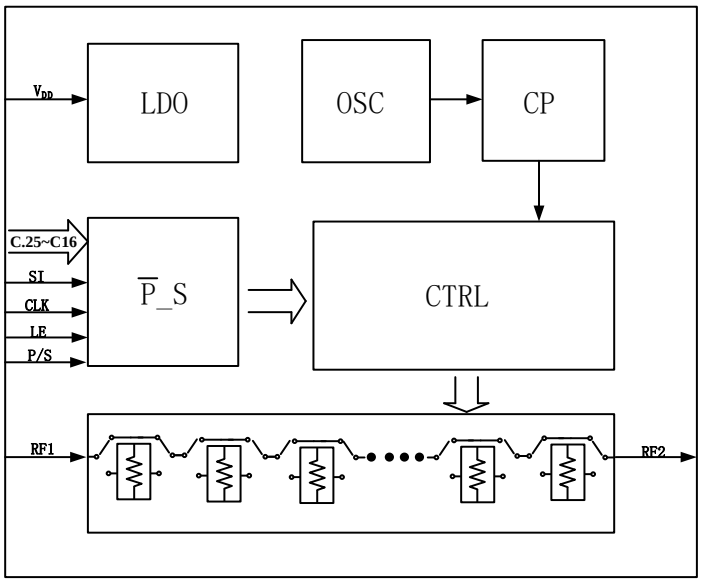
Designation	Package Type	Operating Temperature
X130	QFN24	-40℃～105℃

Scope of Application

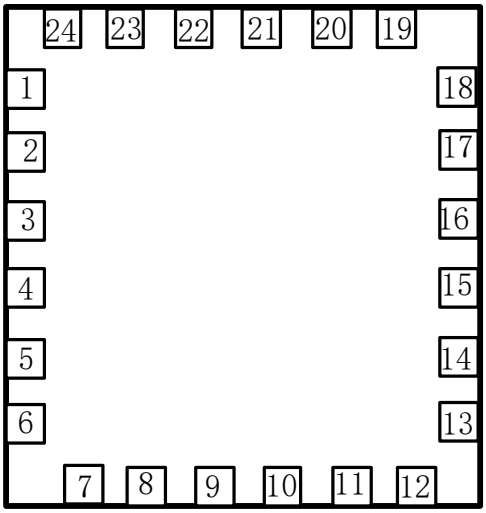
• Wireless communication systems

• RF transceiver systems

Functional Block Diagram



Layout of Pins



Pin Definitions

S/N	符号 Symbol	Description	S/N	Symbol	Description
1	C0.25	Parallel port control, 0.25dB	13	GND	Ground
2	V_{DD}	Power supply	14	RF2	RF output
3	$\overline{P}$ /S	Serial-to-parallel conversion control port (1 is serial input, 0 is parallel input)	15	GND	Ground
4	GND	Ground	16	LE	Latch enable terminal
5	RF1	RF input	17	CLK	Clock input
6	GND	Ground	18	SI	Serial Data In
7	GND	Ground	19	C16	Parallel port control, 16dB
8	GND	Ground	20	C8	Parallel port control, 8dB
9	GND	Ground	21	C4	Parallel port control, 4dB
10	GND	Ground	22	C2	Parallel port control, 2dB
11	GND	Ground	23	C1	Parallel port control, 1dB
12	GND	Ground	24	C0.5	Parallel port control, 0.5dB

Absolute Maximum Ratings

(All voltages are referenced to GND)

Parameter	Min.	Max.	Unit
Supply voltage range		6	V
Control voltage range		6	V
Input signal power		31	dBm

Storage temperature	-65	150	℃
ESD(HBM)		1000	V
ESD(CDM)		500	V

Recommended Operating Conditions

Parameter	Min.	Typical	Max.	Unit
Supply voltage	2.7	3.3	5.5	V
Digital high level	1.1		V_{DD}	V
Digital low level	-0.3		0.7	dBm
Operating temperature range	-40	+25	+105	℃
Max. junction temperature (10-year life)			125	℃

Electrical Characteristics

(Test conditions: except as otherwise herein provided, -40°C≤T_A≤105°C, V_{DD}=3.3V, V_{CTRL}=0V/3.3V, R_{LOAD}=50Ω, P_{IN}=0dBm)

Characteristics	Symbol	Conditions	Parameters			Unit
			Min.	Typical	Max.	
Operating current	Icc		--	180	300	uA
Insertion loss	IL	9KHz~1.0GHz	--	1.1	2.3	dB
		1GHz~2.2GHz	--	1.3	2.7	dB
		2.2GHz~4.0GHz		1.6	3.5	dB
		4.0GHz~5.0GHz		2.1	4.1	dB
		5.0GHz~6.0GHz	--	2.6	4.6	dB
Attenuator step	ATT_{step}		0.25	0.5	1	dB
Attenuation range	ATT_R	0.25dB	0		31.75	dB
		0.5 dB	0		31.5	
		1dB	0		31	
Attenuator error	ATT_{err}	0.25dB step(0~31.75dB)				
		9KHz~2.2GH	--	±(0.15+0.5% of set)	±(0.15+2.5% of set)	dB
		2.2GHz~3GHz	--	±(0.15+1.3% of set)	±(0.15+2.5% of set)	
		3GHz~4GHz	--	±(0.25+2.5% of set)	±(0.25+4.5% of set)	
		0. 5dB step(0~31.5dB)				
		9KHz~2.2GH	--	±(0.15+0.5% of set)	±(0.15+2.5% of set)	dB
		2.2GHz~3GHz	--	±(0.15+1.3% of set)	±(0.15+2.5% of set)	
		3GHz~4.5GHz	--	±(0.25+2.5% of set)	±(0.25+4.5% of set)	

		4.5GHz~5GHz	--	±(0.25+4.2% of set)	±(0.25+4.5% of set)	
		1dB step(0~31dB)				
		9KHz~2.2GH	--	±(0.15+0.5% of set)	±(0.15+2.5% of set)	dB
		2.2GHz~3GHz	--	±(0.15+1.3% of set)	±(0.15+2.5% of set)	
		3GHz~4.5GHz	--	±(0.25+2.5% of set)	±(0.25+4.5% of set)	
		4.5GHz~5GHz	--	±(0.25+4.2% of set)	±(0.25+4.5% of set)	
		5GHz~5.5GHz	--	±(1 +3.5% of set)	±(1+5% of set)	
		5.5GHz~6GHz	--	±(1 +6.5% of set)	±(1+9% of set)	
Input return loss	S_{11}	9KHz~5GHz	10	12	--	dB
		5GHz~6GHz	9	11	--	
Output return loss	S_{22}	9KHz~5GHz	10	14	--	dB
		5GHz~6GHz	9	12	--	
Switching speed	Tsw	50% CTRL to 10% or 90% RF	--	70	100	ns
Input Third-order Intercept Point	IIP3	9KHz~4.0GHz ， Pin=18dBm/tone, 20MHz Spacing	50	55	--	dBm
		4.0GHz~5.0GHz ， Pin=18dBm/tone, 20MHz Spacing	43	50	--	
		5.0GHz~6.0GHz ， Pin=18dBm/tone, 20MHz Spacing	41	45	--	
Input 1dB compression point	P_{-1}	9KHz~4.0GHz	30	31	--	dBm
		4.0GHz~5.0GHz	25	30	--	
		5.0GHz~6.0GHz	23	29	--	
Switch glitch	Glitch	Greater than 100ns after gain switching	--	0.03	0.3	dB
Spurious signals	Spur	＜100MHz	--	-95	-90	dBm
		100MHz~6GHz	--	-115	-110	
Delay	Delay		--	5	10	ns
Initial power-on delay difference between different chips at different attenuation levels	△Delay	＜3GHz	--	0.05	0.1	ns

Initial power-on phase difference between different chips at different attenuation levels	△Phase	＜3GHz	--	2	5	°
Consistency of phase change between different chips at different attenuation levels	$\triangle Phase_{14dB}$	Phase difference between any attenuation level and 14dB,＜3GHz	--	1	1.25	°
Phase difference between any attenuation level and 8dB	$\triangle Phase_{8dB}$	＜3GHz	--	11	12	°
Phase difference between 5°C	$\triangle Phase_{5℃}$	Same attenuation	--	0.9	1	°
Stabilization time	t	Signal fluctuation is less than 0.05 dB	--	1	1.5	us

Control Logic

1. Parallel/Direct Port

The parallel port is provided with 7 control ports, and the truth table in the parallel/direct operation mode is shown in Table 1. In the parallel operation mode, the serial control ports CLK and SI should be grounded.**Table1**

Table1. Truth Table in Parallel Control Mode

并行控制设置 Parallel control settings							衰减值 Attenuation
C16	C8	C4	C2	C1	C0.5	C0.25	
L	L	L	L	L	L	L	Reference IL
L	L	L	L	L	L	H	0.25dB
L	L	L	L	L	H	L	0.5dB
L	L	L	L	H	L	L	1dB
L	L	L	H	L	L	L	2dB
L	L	H	L	L	L	L	4dB
L	H	L	L	L	L	L	8db
H	L	L	L	L	L	L	16dB
H	H	H	H	H	H	H	31.75dB

For Latched Parallel programming,, the rising edge of the LE signal acquires data, outputs data at a high level, and latches data at a low level.

For Direct Parallel programming, the LE signal is to be sent to a high-level terminal. Changing the attenuation control value can change the attenuation accordingly. The temporal structure in the parallel/direct mode is shown in Figure 1.**Figure 1**

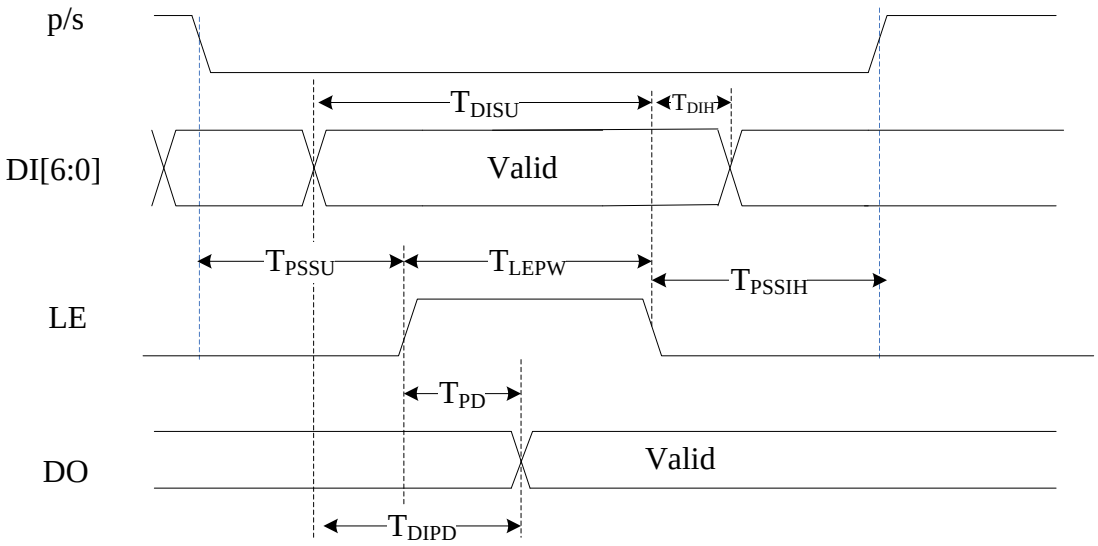


Figure 1 Temporal Structure in the Parallel/Direct Mode

Table 2 AC Characteristics in the Parallel and Direct Modes

Parameter	Min	Max	Unit
Min. electrical pulse width of the Latch enable signal T_{LEPW}	30		ns
Serial data setup time T_{DISU}	100		ns
Serial data hold time T_{DIH}	100		ns
Serial-parallel selection signal setup time T_{PSSU}	100		ns
Serial-parallel selection signal hold time T_{PSIH}	100		ns
Digital register delay T_{PD}		10	ns
Digital register delay (direct mode) T_{DIPD}		5	ns

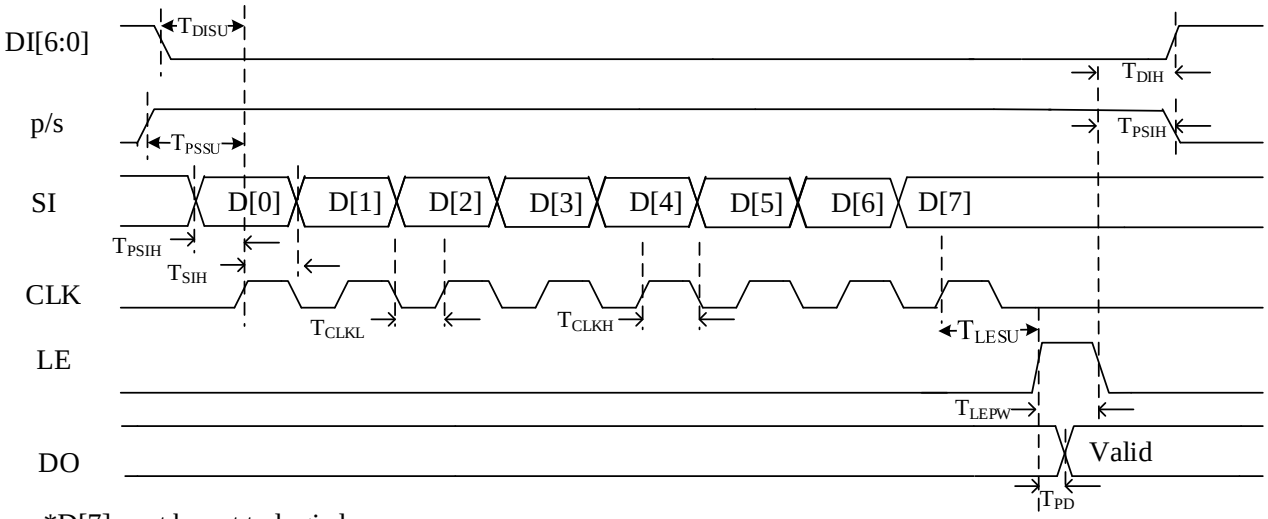
2. Serial Mode

Table 3In the serial operation mode, the parallel control ports C0.25 ~ C16 should be grounded.

Table 3 Truth Table In Serial Mode

	串行控制设置 Serial control settings							衰减值 Attenuation
D7	D6	D5	D4	D3	D2	D1	D0	
L	L	L	L	L	L	L	L	Reference IL
L	L	L	L	L	L	L	H	0.25dB
L	L	L	L	L	L	H	L	0.5dB
L	L	L	L	L	H	L	L	1dB
L	L	L	L	H	L	L	L	2dB
L	L	L	H	L	L	L	L	4dB
L	L	H	L	L	L	L	L	8db
L	H	L	L	L	L	L	L	16dB
L	H	H	H	H	H	H	H	31.75dB

The serial port is controlled by the SI, Clock and LE signals. The rising edge of the Clock signal acquires the data of the SI signal. The serial data sequence is LSB first. The shift register loads data when the LE signal is at a low level. After the data is loaded, the LE signal shifts its low level to a high level. When the LE signal is at a high level, the shift register outputs data. The temporal structure in the serial mode is shown in Table 1.**Table1**



*D[7]must be set to logic low

Figure 2 Temporal Structure in the Serial Mode

Table 4 AC Characteristics in the Serial Mode

Parameter	Min	Max	Unit
Serial clock frequency F_{CLK}		10	MHz
Serial clock HIGH,T_{CLKH}	30		ns
Serial clock LOW,T_{CLKL}	30		ns
From the rising edge of the last serial clock signal to the rising edge of the LE signal, T_{LESU}	10		ns
Min. pulse width of the LE signal, T_{LEPW}	30		ns
Serial data setup time, T_{SISU}	10		ns
Serial data hold time, T_{SIH}	10		ns
Parallel data setup time, T_{DISU}	100		ns
Parallel data hold time, T_{DIH}	100		ns
Serial-parallel selection signal setup time TPSSU	100		ns
Serial-parallel selection signal hold time TPSIH	100		ns
Digital register delay T_{PD}		10	ns
V_{DD}=3.3V or 5V, -40℃<T_A<+105℃			

Test Curve

Test conditions: Except as otherwise herein provided, T_A= 25°C and V_{DD}=3.3V, Z_S=Z_L=50Ω

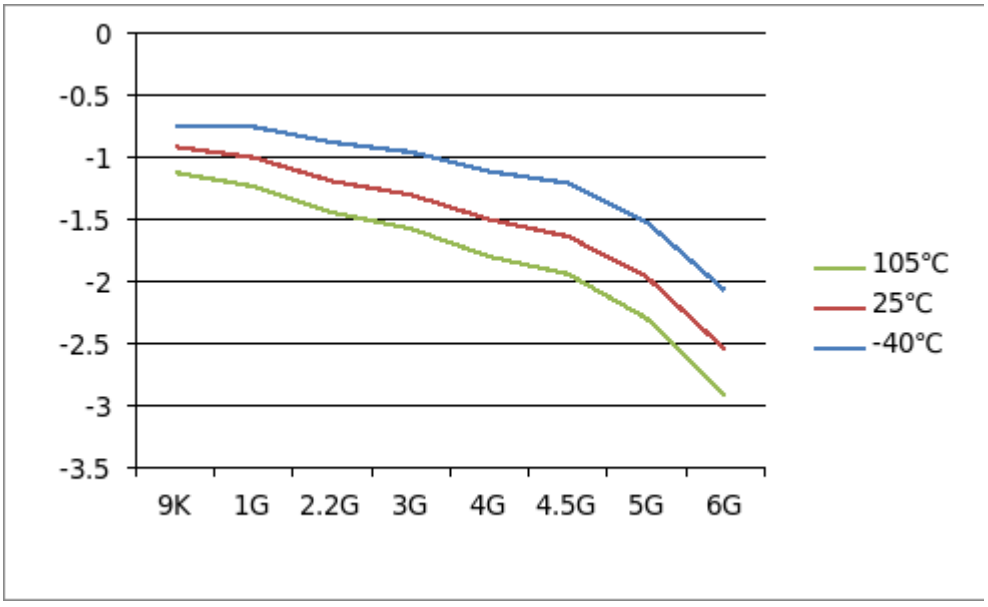


Figure 3 Insertion Losses

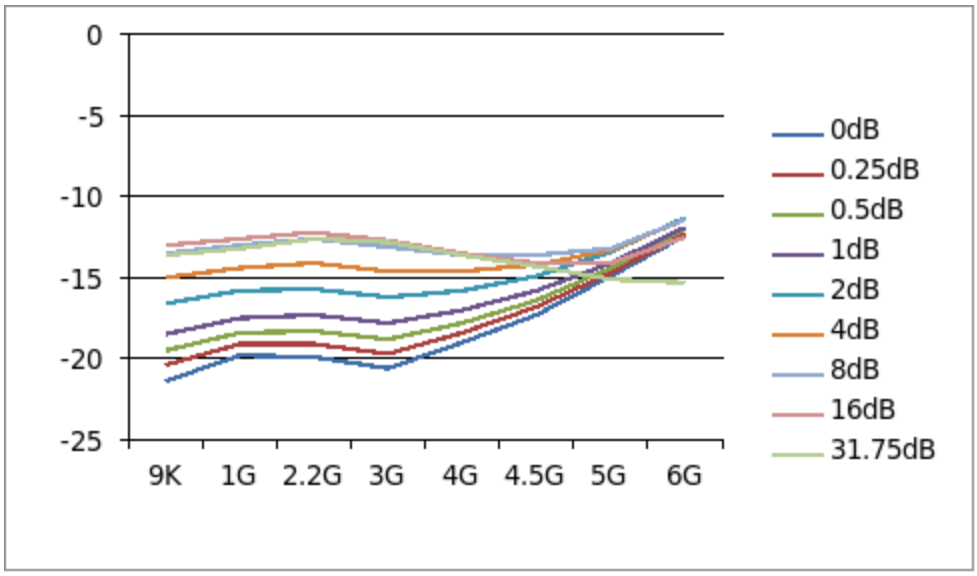


Figure 4 Input Return Losses

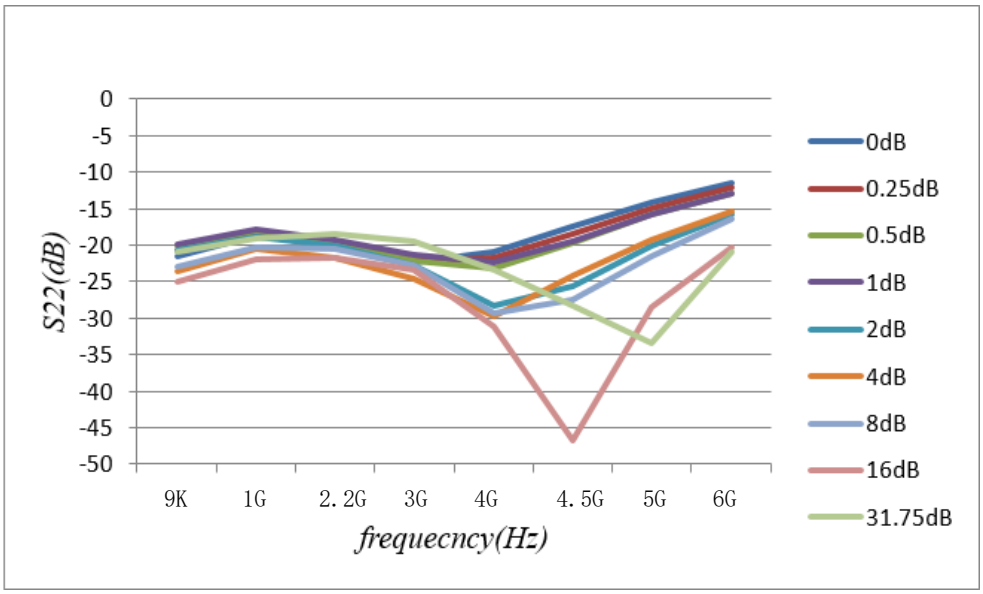


Figure 5 Output Return Losses

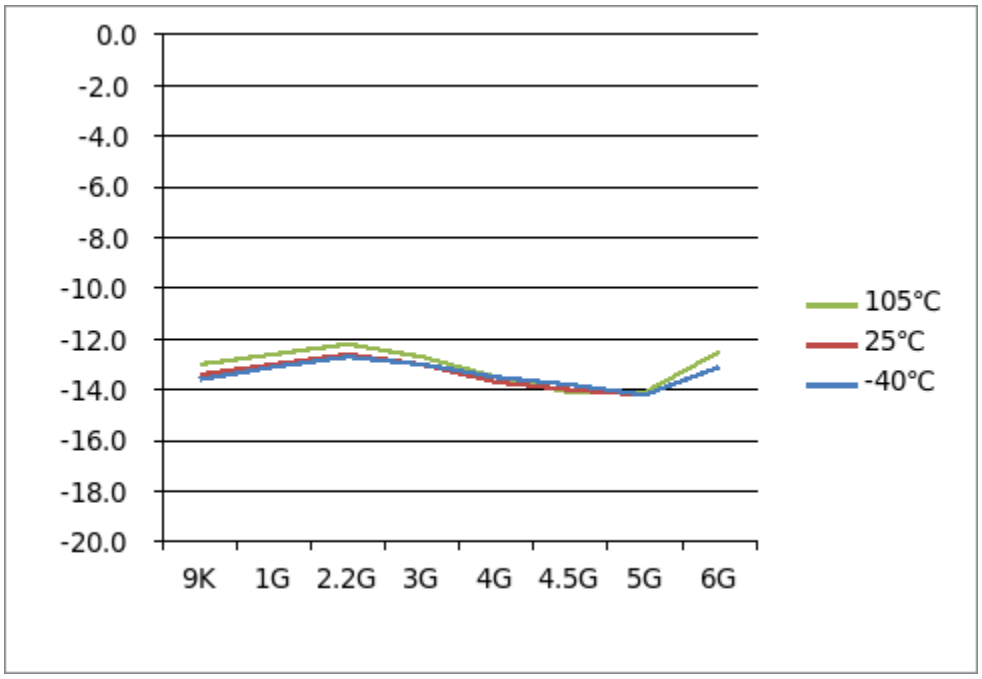


Figure 6 Input Return Losses at 16dB

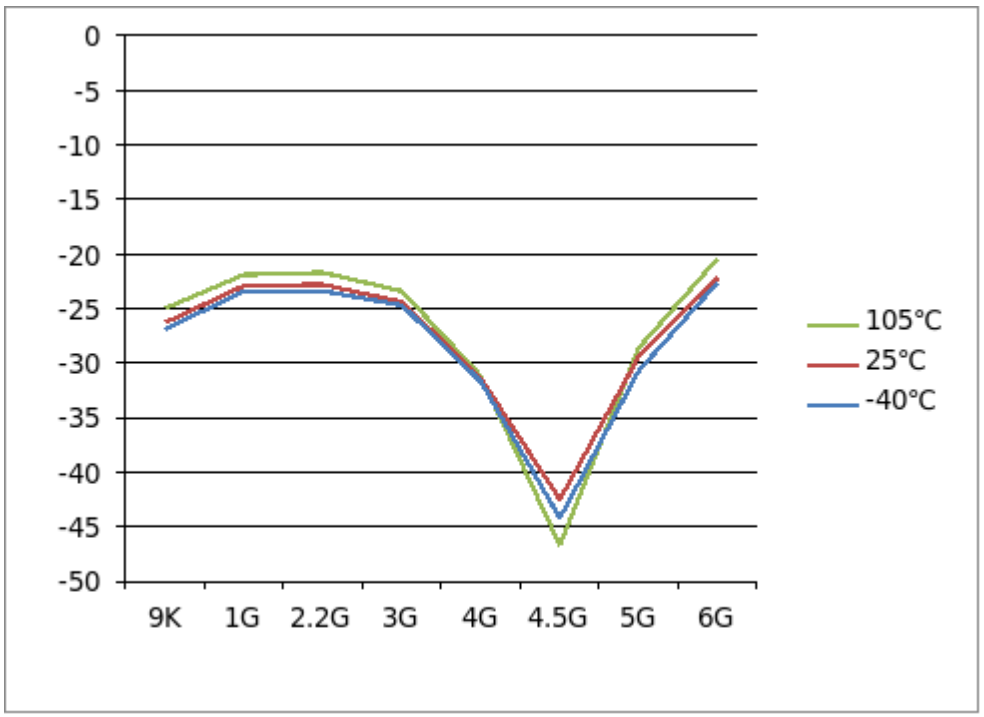


Figure 7 Output Return Losses at 16dB

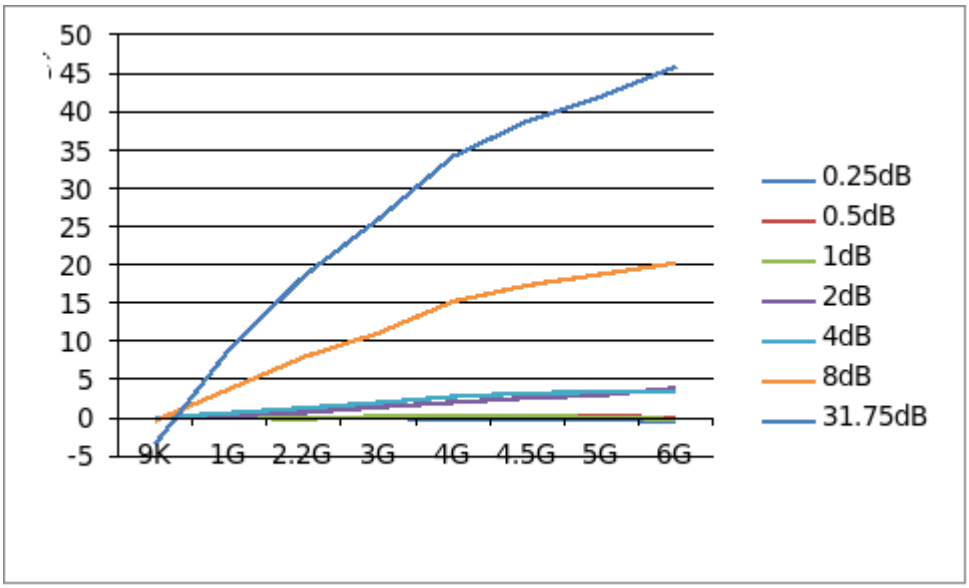


Figure 8 Additional Phase Shift VS Main Attenuation

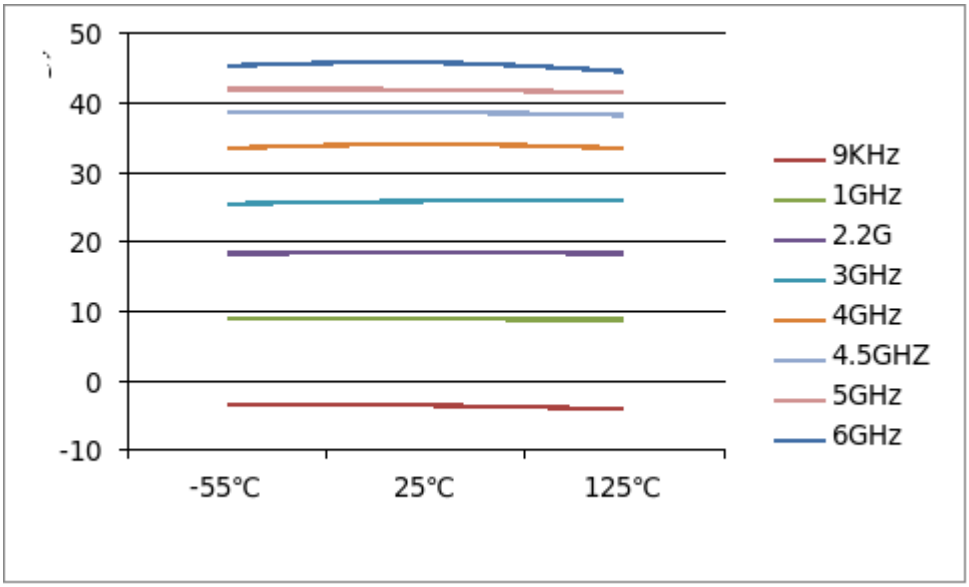


Figure 9 Additional Phase Shift at 31.75dB VS Temperature at Different Frequencies

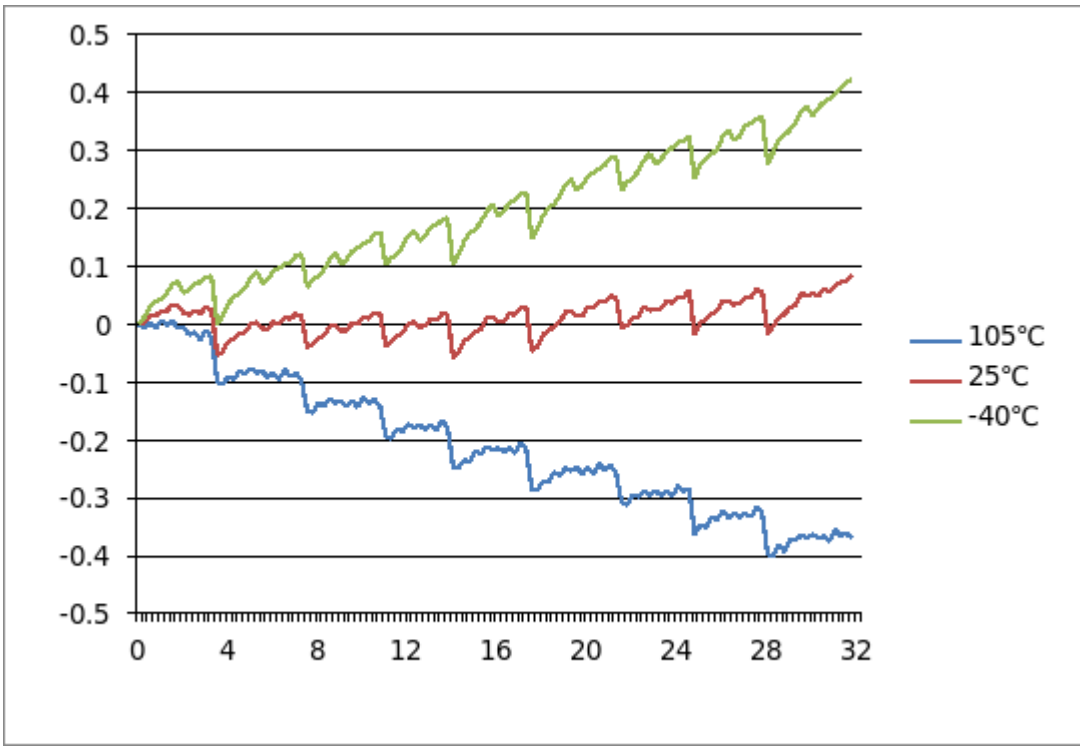


Figure 10 Attenuation Error at 900KHz VS Temperature

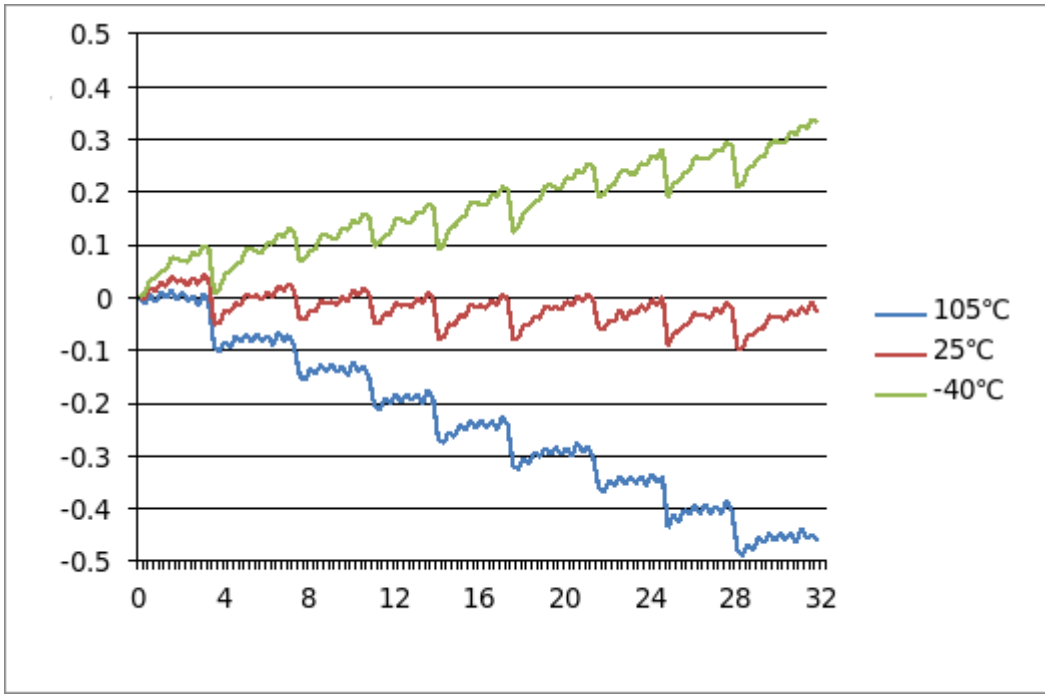


Figure 11 Attenuation Error at 1000MHz VS Temperature

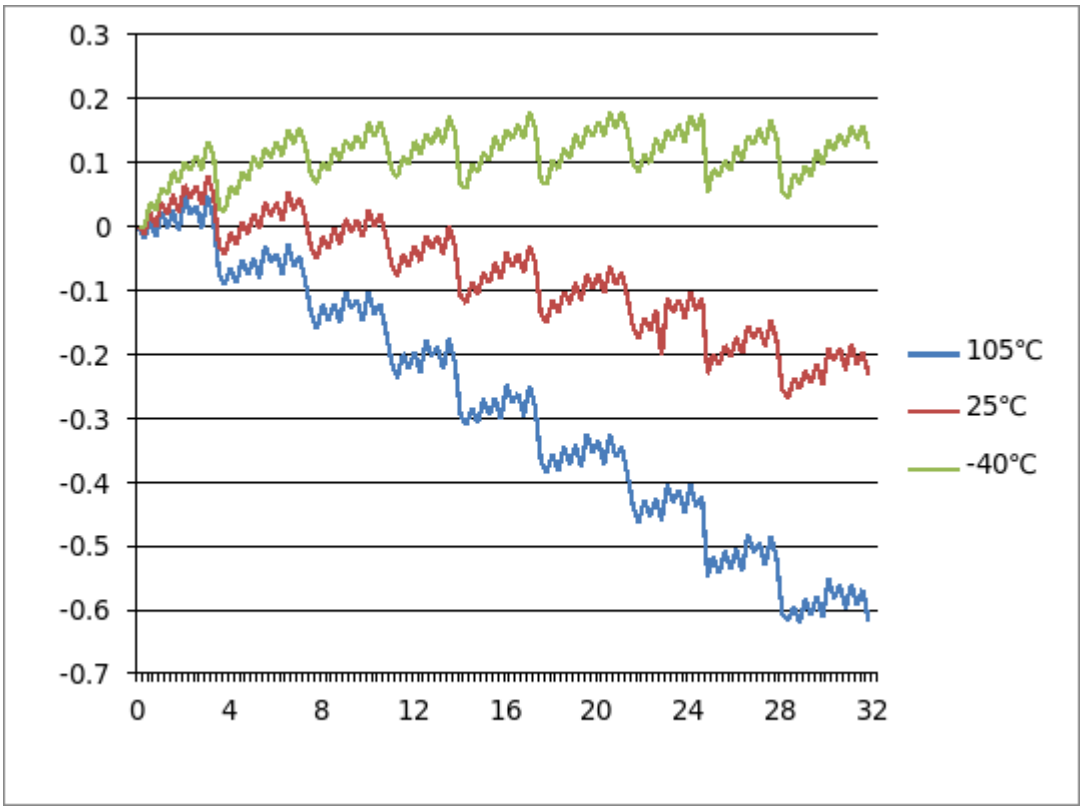


Figure 12 Attenuation Error at 2200MHz VS Temperature

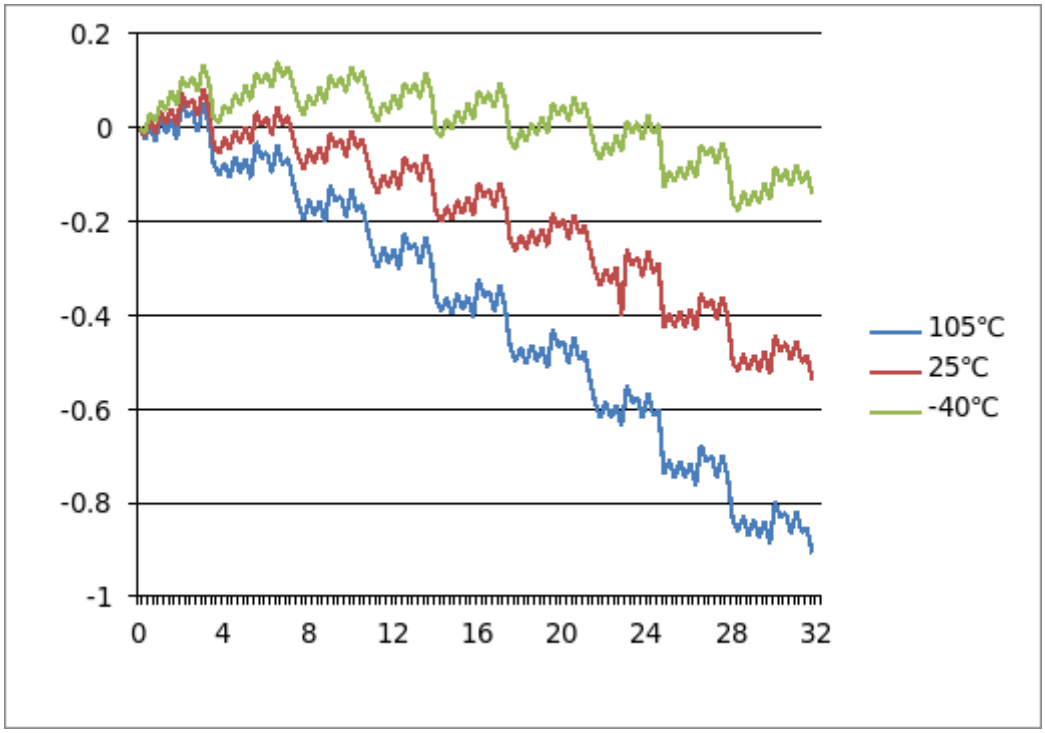


Figure 13 Attenuation Error at 3000MHz VS Temperature

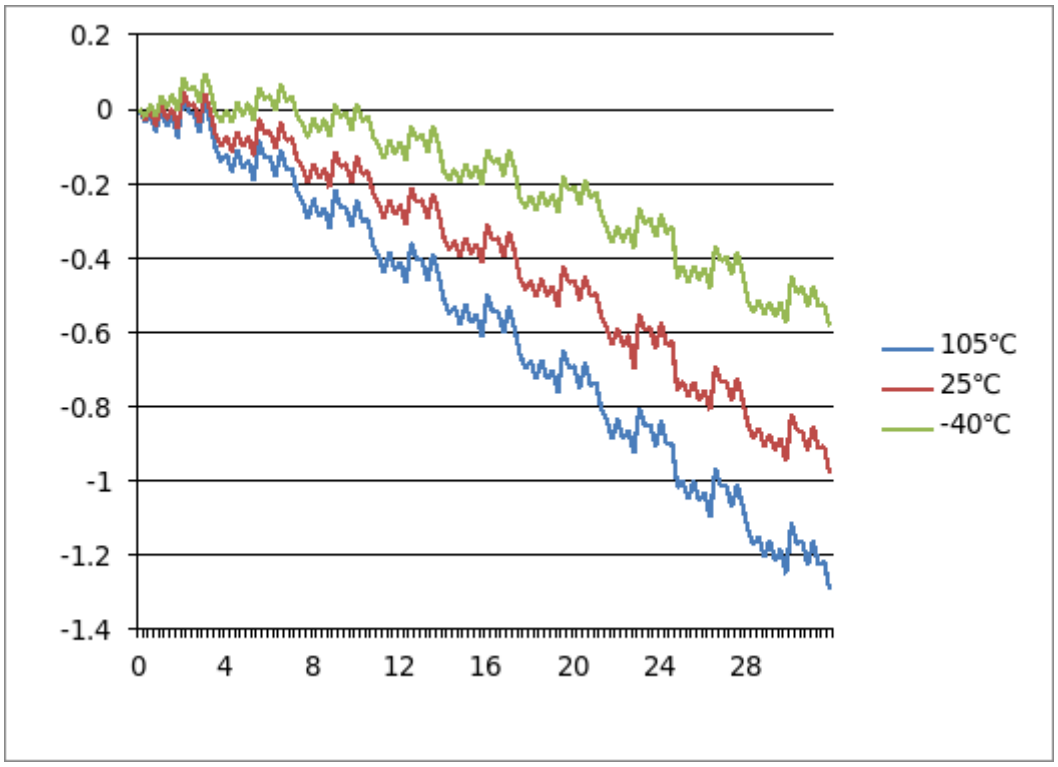


Figure 14 Attenuation Error at 4000MHz VS Temperature

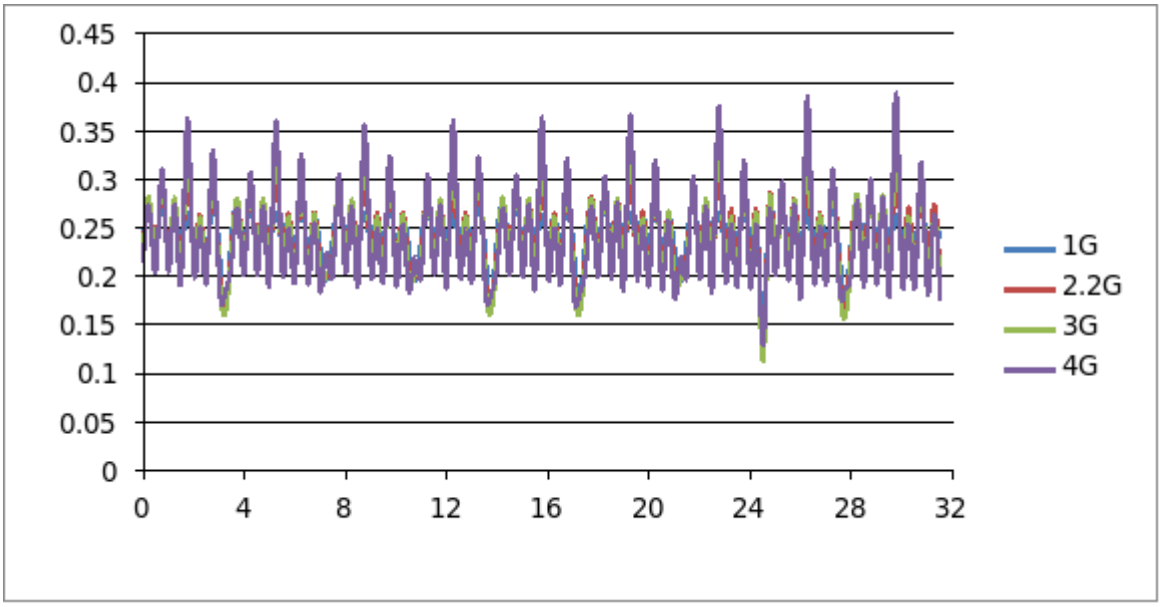


Figure 15 Step Error VS Frequency (at 0.25dB Step)

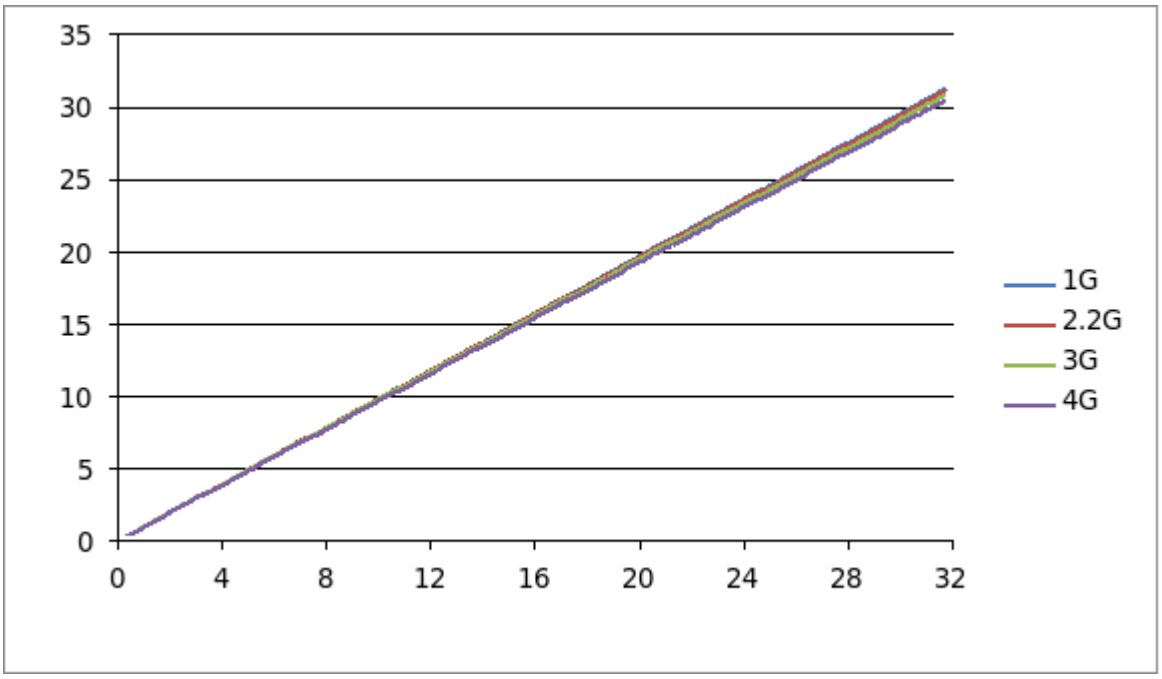


Figure 16 Comparison of Actual Attenuation and Ideal Attenuation (at 0.25dB Step)

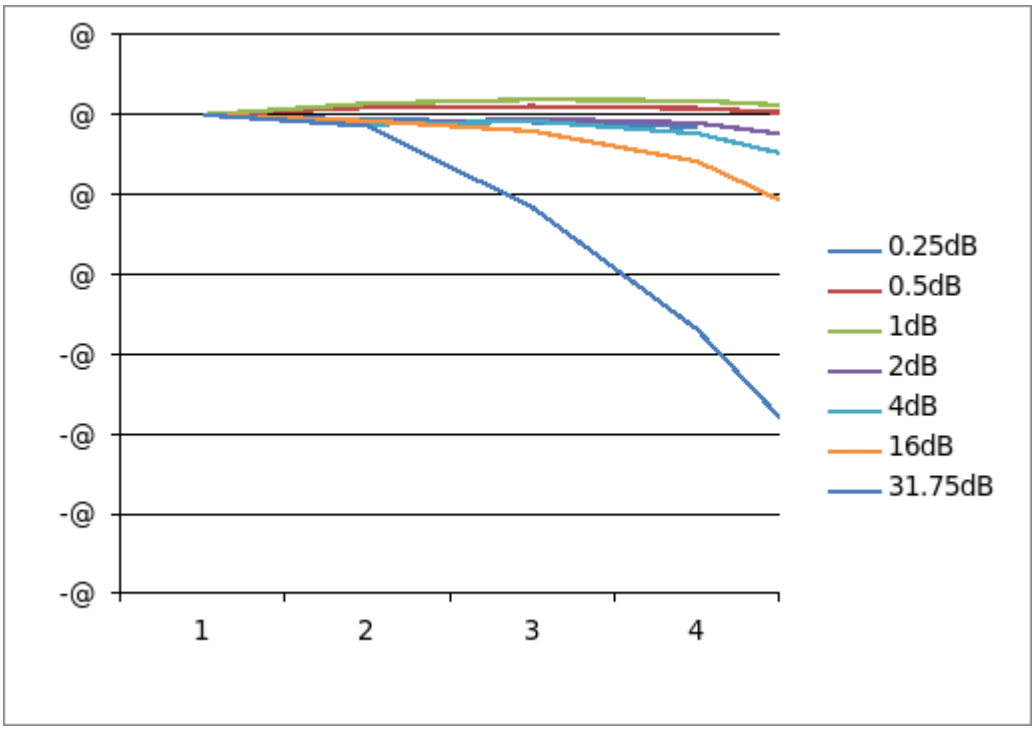


Figure 17 Main Step Attenuation Error VS Frequency (at 0.25dB Step)

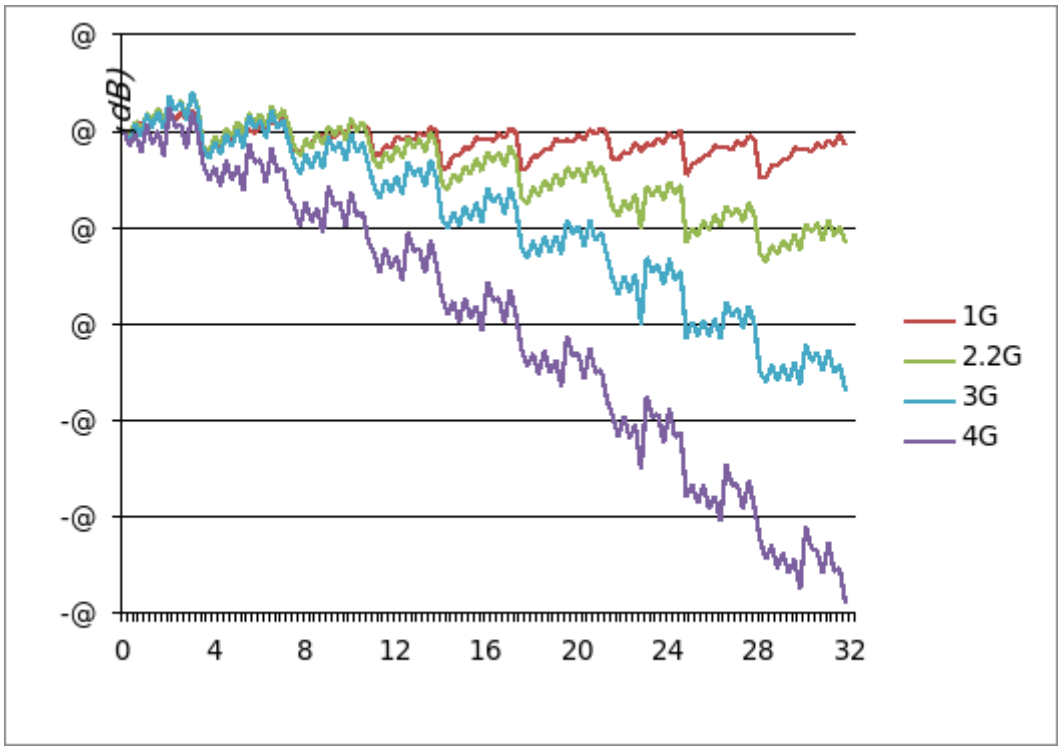


Figure 18 Attenuation Error VS Frequency (at 0.25dB Step)

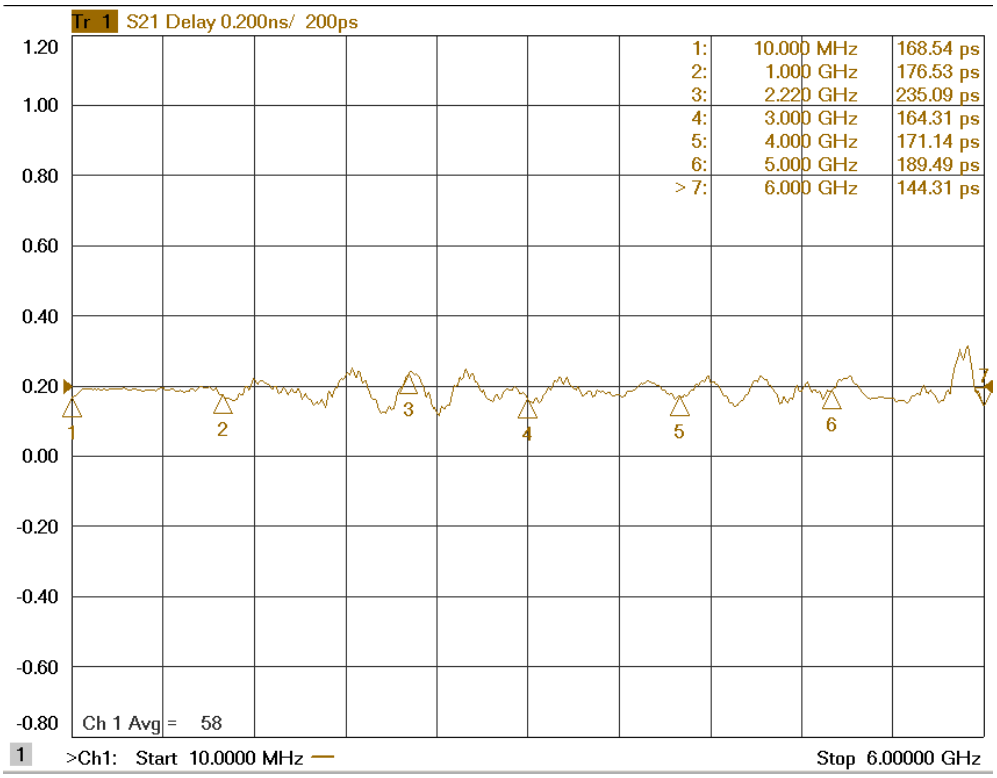
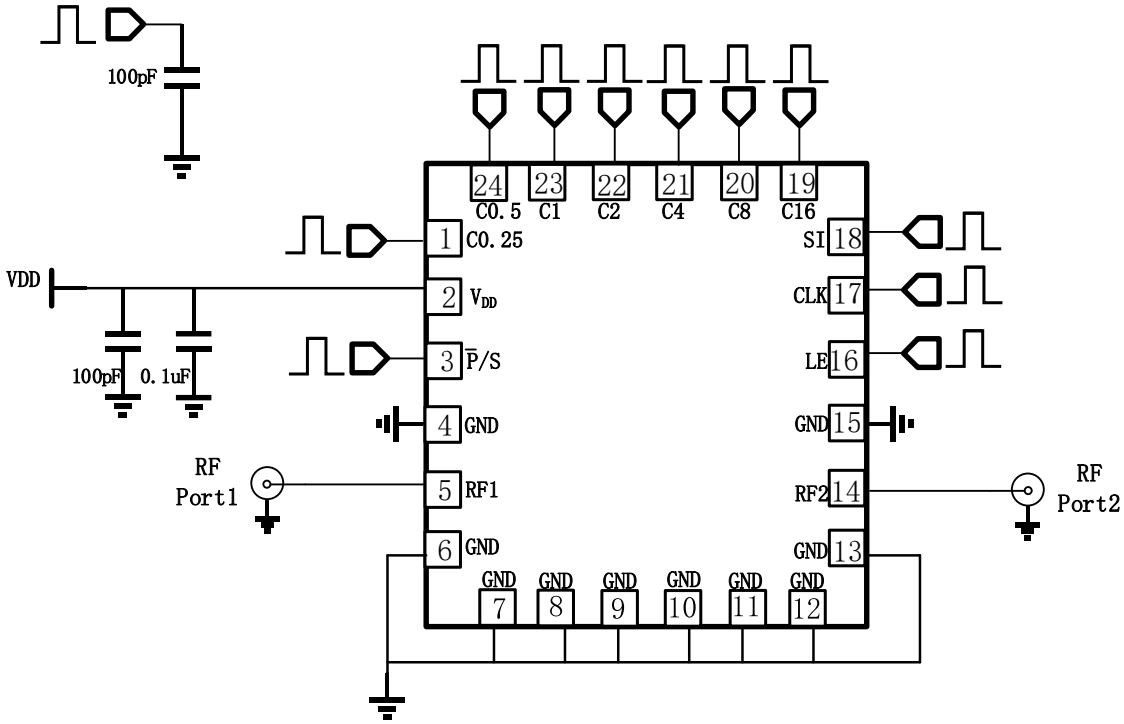


Figure 19 Delay VS Frequency

Typical Applied Circuit



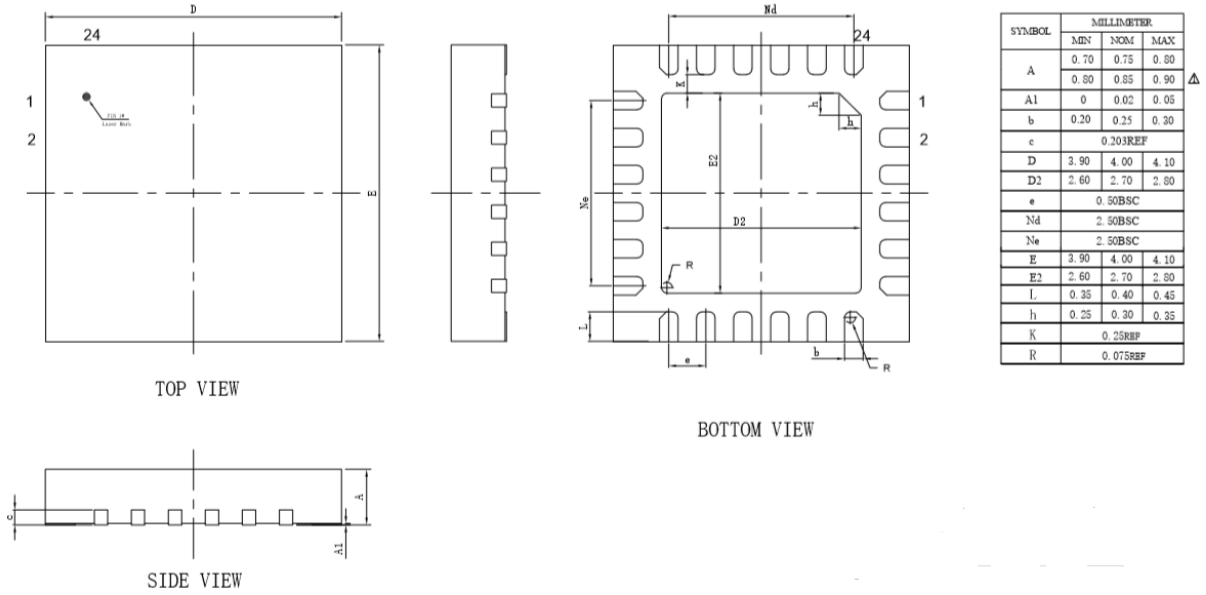
Notes: 1. When the voltage of all DC operating points of the peripheral circuit is 0V, no blocking capacitor is required for each RF port.

2. When the voltage of all DC operating points of the peripheral circuit is not 0V, a blocking capacitor is required for each RF port.

3. A 200K pull-down resistor is built in each of the control ports C0.5~C16, SI, CLK and$\bar{P}$/S.

4. A 300K pull-up resistor is built in the control port LE.

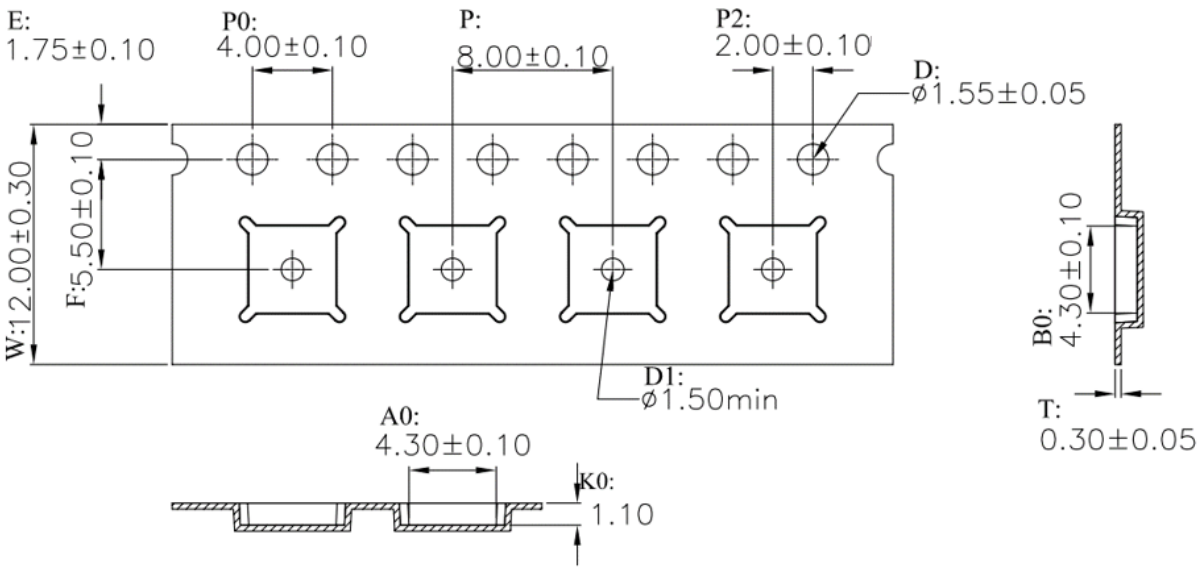
Package Outline



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.20	0.25	0.30
c	0.203REF		
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e	0.50BSC		
Nd	2.50BSC		
Ne	2.50BSC		
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
L	0.35	0.40	0.45
h	0.25	0.30	0.35
K	0.25REF		
R	0.075REF		

Figure 20 X130 Package Outline

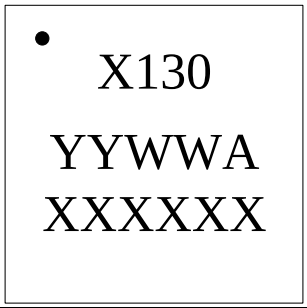
Reels of Package



1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 19" reel : 500.0 Meters.(復卷)
7. Component load per 13" reel : 5000 pcs.

Figure 21 Reels of Package

Product Identification Image and Pictures



Code	Description
X130	号 Model
YYWWA	Year and week, where YY indicates the last two digits of the year, WW is the week, A is the wafer number, A=1 #, B=2 #, C=3 #... and so on
XXXXXX	… LOT ID No., e.g., 1923A for the 1# wafer F31630 (LOT ID No.) packaged in the 23rd week of 2019, and 1923B for the 2# wafer F31630...

Moisture Sensitivity Level

X130 is available in a 24-pin 4×4 mm QFN package at a Moisture Sensitivity Level (MSL) 3.

Notes

1. Grounding: The metal base should be grounded with as many through holes as possible to reduce parasitic inductance.
2. The amplifier should be adopted according to the recommended typical applications.
3. Electrostatic discharge (ESD) damage protection: The amplifier is an ESD-sensitive device, and adequate ESD countermeasures should be taken during transmission, assembly and testing accordingly.
4. The Product Specification shall be subject to the date of release and shall be modified in due course without further notice.

Storage Conditions

1. The product is at a Moisture Sensitivity Level (MSL) 3, so it should be stored and used in accordance with the appropriate regulations of MSL 3.

Version Information

Version No.	Creation Date	Description	Page Changed
Rev 0.1	2020.2.18	Pre-release	
Rev 0.2	2020.6.19	Pre-release	P3
Rev 1.0	2020.9.25	： Official release:	P1、P3、P4、P7~ P17

		2. Update the block diagram of the product; 4. Update product specifications; 6. Update the test curve; 8. Add product identification images.	
Rev 1.1	2021.01.28	Add information about reels of the package and update the storage condition	P18、P19